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Website: Kjar.spu.edu.iq | Email: kjar@spu.edu.iq

Mitigation of Harmonics and Unbalanced Voltage Disturbance Compensation by MSVPWM Based- DVR in the Distribution Net

Haider Muhamad Husen

Electrical Department

Kalar Technical College

Sulaimani Polytechnic University

Sulaimani, Iraq

haider.husen@spu.edu.iq

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ABSTRACT

Recent power distribution networks comprise abundant sensitive loads, which extremely impact the power quality of source in electrical power networks. Voltage dip, voltage rise, imbalanced voltage, line notching and distortion of harmonics are problems of power quality frequently take place. Pre-disturbance voltage compensation strategy and phase-locked-loop (PLL) based dq-space vector control are presented to improve a Dynamic Voltage Restorer (DVR), which restore the magnitude of voltage disturbance and displacement of phase angle to prior of voltage disturbance. 3-phase Multilevel strategy of Space Vector Pulse Width Modulation (MSVPWM) based- Multilevel Diode Clamped Converter (MDCC) is proposed as switching pulse signals employed low frequency, which creates high levels of voltage and fewer harmonics in the output waveform in comparison to 2-level SVPWM based- DVR. 3-level SVPWM based- DVR under balanced and imbalanced distortion voltage disturbances included sags and swells injected appreciated quantities of voltage, thereby attained ideal sinusoidal waveform with lower Total Harmonic Distortion THD% compared to 2-level SVPWM based- DVR. Furthermore, real and imaginary powers balanced effectively at sensitive load during various distortion voltage disturbance conditions via presented work. The proposed simulation model of multi-level SVPWM based-DVR is implemented by dedicating the software system of MATLAB/SIMULINK. The results of simulation exhibit the effectiveness and efficiency of the presented work under different distortion voltage disturbance conditions.

1. INTRODUCTION

The capability of power distribution networks to supplied uninterrupted electric power at the ideal waveform of voltage with nominal amplitude and frequency are concerning to power quality [1]. As a result of copious sensitive equipment in the distribution systems, the disturbances of power quality like supply voltage sag, line swell, transients, and harmonics are created and they lead to effect on customer loads, mis-operation, and economical losses [2]. The multiple of frequency of the supply system is called harmonics [3]. Among various disturbances in the distribution network, sags of voltage compared to other issues of power quality are most frequently taken place. Consequently, results huge losses of power at the various loads of customer [4]. Voltage dip is an instantly reduction in magnitude of root mean square voltage ranges 10% through 90% of rated value with time duration at the fundamental frequency between 0.01 sec to 1 minute. Voltage rise, in contrast, is an increase in value of root mean square voltage rapidly compared to nominal value from 110% to 180% that lasts time duration through 0.01 sec to 1 minute [5]. In the source voltage of 3-phase power system, when the peak of voltages are not symmetrical and also phase shift is not (120°), then the system of 3-phase power supply called unbalanced voltage [3]. Customer power devices are employed to ameliorate the quality of the distribution system in the electrical power networks [6]. Among different customer power devices, the DVR is superior performance and most efficient on account of its merits encompass smaller size, least cost, and rapid response [7]. Power electronic devices based- DVR is utilized to compensate voltage disturbances by the injection of the desired three phase voltages which is synchronized via PLL, and in series with the power distribution feeders [8]. Space vector pulse width modulation strategy is preferred as compared to sinusoidal PWM in VSI consequence of simplicity and easily implementation for digital controller. Further, switching losses reduction, best exploited for DC- voltage, and created least harmonics are SVPWM feature with VSC [9-10]. With 2-level space vector PWW the THD% is less than sinusoidal PWM and switching losses are reduced as a result of voltage change in only one phase every time [11]. Multi-level SVPWM technique based-neutral point diode clamped converter in comparison with 2-level SVPWM method with same low value of switching frequency reduces the stress of voltage on any switch and create least harmonics at the output voltage signal [12]. Reduction of THD% is achieved by improved switching sequence for 3-level diode clamped converter of multilevel space vector PWM technique [13]. Simulation results of multi-level diode clamped converter with direct torque control (DTC) of 3-phase induction motor (IM) are compared with 2-level converter under various speed condition with different loads [14]. Optimized switching sequence of multi-level neutral point diode clamped converter compared with conventional space vector PWM fed 3-phase induction motor, by means of that percent of THD reduced significantly with improved switching sequence of SVPWM [15]. Field oriented control (FOC) and direct torque control (DTC) controlled multi-level neutral point diode clamped converter fed Interior Permanent Magnet Synchronous Motor for application of Electric Vehicle (EV). Consequently, performance of torque/speed characteristic improved and reduction of harmonics observed [16]. Three-level SVPWM based multi-level diode clamped converter employed as control strategy for energy management with application of multi-source system, thereby simulation results showed control of variables are achieved by this strategy [17]. In this paper simulation work is presented. The pre-disturbance voltage compensation strategy [18] is employed with DVR and Phase-Locked-Loop [19] based- DQ space vector controller [20] is presented to detect voltage disturbances and determines the reference signals for three phase voltage independently. To validate the efficiency and effectiveness of the presented PLL based- dq-vector control with DVR, MATLAB/SIMULINK software program is dedicated.

2. FUNCTIONS AND POSITION OF THE DYNAMIC VOLTAGE REGULATOR

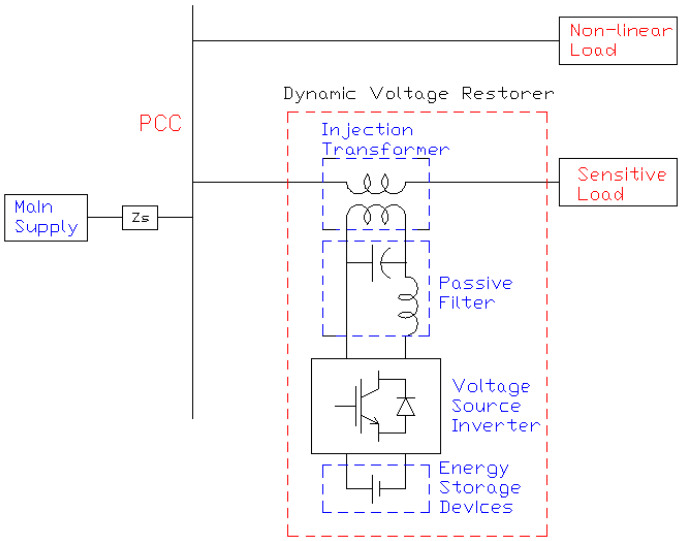


Figure 1: Position and elements of the series voltage restorer

The dynamic voltage controller as shown in Fig.1 interface at a PCC between the power supply source and the feeder of the sensitive load, which is essentially VSI and capable to inject/absorb additional real and imaginary power to/from the distribution network to avoid sensitive load from tripping by compensating of voltage dip/rise via injecting voltage in series with main source [21].

2.1 Injection Step-up Transformer

The compensated voltage is provided into the lines of distribution network by injection step-up transformer, which interfaces the DVR with the distribution network through the secondary winding and convert the output voltage of VSI to the main source voltage when the voltage disturbance takes place which is detected by the controller. Further, isolating of DVR from the power system is achieved by booster step-up transformer.

2.2 Frequencies Filter

A harmonic filter exploited capacitor and inductor as a passive filter, which is located between the voltage source converter and low-voltage terminal of booster transformer to eliminate the components of harmonics as a result of pulse width modulation technique employed with VSI.

2.3 Devices of Energy Storage

Storage devices as super capacitors, super conducting magnet (SCM) energy storage, flywheels, and batteries are employed to provide the appreciated real power during the voltage disturbances. The efficient of the DVR is depended on the compensation quantity of the real power provided from the storage devices.

2.4 IGBT Based- Three-phase Voltage Source Converter

The controllable electrical power supply, comprised amplitude and frequency of three phase voltages inverted from devices of energy storage or via rectifier devices by employed pulse width modulation techniques as switching signals called VSI, must be capable to operate under imbalanced three phases voltage independently due to the voltage disturbances in power system network which are mainly unbalanced and accompanied with a displacement of phase angle.

3. VARIOUS STRATEGIES WITH PROPOSED CONTROL FOR DVR

The proposed scheme of control strategies based on dq- coordinate transformation to implement and improve the performance of DVR is depicted in Fig. 2.

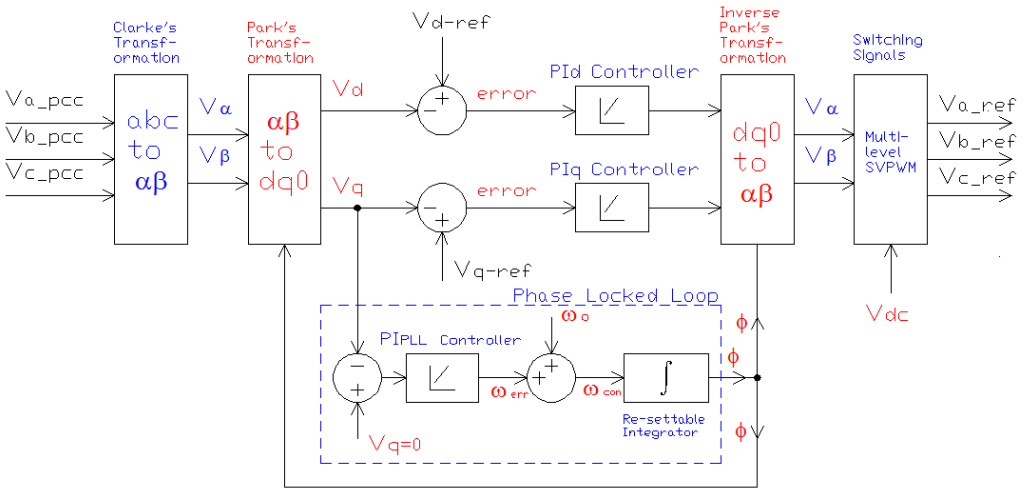


Figure 2: Control strategy scheme for DVR

3.1 Voltage Disturbance Compensation Techniques

Various techniques presented to restore the peak values with phase angle displacement of the sensitive load voltage by the DVR to prevent tripping [18].

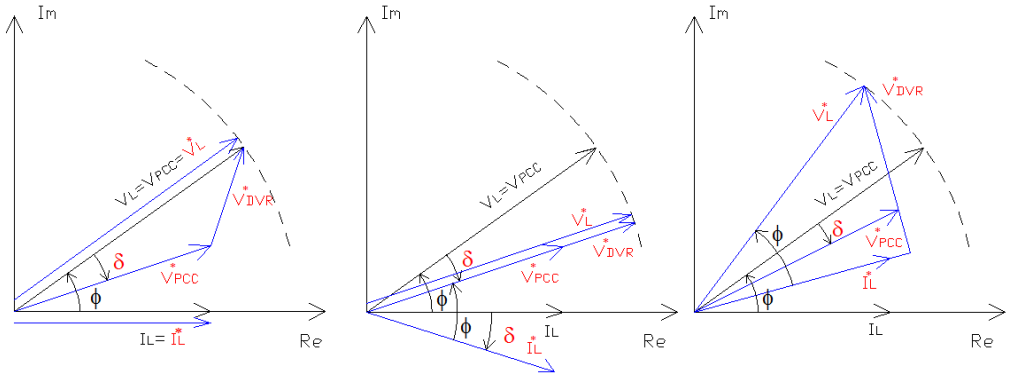


Figure 3: Various strategies for voltage compensation: (a) Pre-disturbance. (b) In-phase. (c) Minimized-energy.

3.1.1 *Pre-disturbance Voltage Compensation Technique*

The pre-fault compensation technique is depicted in Fig. 3.a, where the vectors $(V_{PCC}, V_L, and\ I_L)$ interpreted pre-fault quantities of point of common coupling voltages, load voltage, and load current respectively, while the phasor voltage $(V^*_{PCC}, V^*_L, V^*_{DVR}, and\ I^*_L)$ represented post-fault quantities of point of common coupling voltages, load voltage, dynamic voltage restorer voltage, and load current respectively. In this technique, synchronized is achieved with the sensitive load voltage by exploited a phase-Locked Loop, thereby the phase angle restored as soon as a disturbance takes placed. Consequently, the peak values and phase

angle of sensitive load voltage is sustained during the disturbance, by means of that least distortion that appeared at the load voltage. This technique is capable to compensate various disturbances comprises symmetrical and unsymmetrical voltage disturbances with and without phase displacement in individual phase voltage utility.

3.1.2 *In-phase Voltage Compensation Technique*

As demonstrated by Fig. 3.b. Compensated voltage magnitude by DVR is minimized by applied in-phase compensation technique compared to pre-disturbance compensation technique. Unlike to pre-fault compensation technique, the compensation technique of voltage in this strategy is in-phase with the utility magnitude of voltage via applied PLL to renew the voltage after the disturbance, whereas the phase displacement remained without compensation, thereby lead to distortion at load. Consequently, in-phase compensation technique is not preferred with DVR to compensate voltage disturbance if there are different of phase variation for utility voltage.

3.1.3 *Energy-minimized Voltage Compensation Technique*

The injected voltage by DVR is controlled to making (90°) with the currents drawing from the load to compensate the disturbances by the injected reactive power as illustrated in Fig. 3. c. Consequently, decreasing the quantity of real power required from the unit of energy storage, thereby energy minimized compensation technique absorbing as much reactive power as possible from the utility. Parallels the advantage of minimizing a real power, phase variation and high quantity of compensated voltage by DVR became major drawbacks of this technique. In this work, the pre-disturbance compensation technique is presented as a result of superior performance during phase variation and the capability of compensation under various voltage disturbances.

3.2 dq-coordinate Transformation (SRF) Based- Phase Locked Loop (PLL)

Issues of power quality as unsymmetrical voltage, line sag, voltage swell, line-notching, harmonics, and phase deviation are the results of interfacing power electronic devices with the main power grid. The dq-SRF based- PLL is capable to pass-up this origin of fault, thereby sustain the phase-lock with the voltage of utility. To accurately estimate the difference of phase angle $(\theta - \phi)$ between the actual angle (θ) and the estimated angle (ϕ) of PLL, the dq-theory is employed as a based- PLL [22]. In electrical power system, symmetrical signals of three-phase are defined as in equation (1)

$$\begin{bmatrix} V_a^{pcc} \\ V_b^{pcc} \\ V_c^{pcc} \end{bmatrix} = |V| \begin{bmatrix} cos(\theta) \\ cos(\theta - \frac{2\pi}{3}) \\ cos\left(\theta - \frac{4\pi}{3}\right) \end{bmatrix} \quad (1)$$

Alpha-beta transformation well-known Clarke's transformation is applied to transform balanced three-phase signal into 2-phase time-varying signals as shown in equation (2)

$$\begin{bmatrix} V_\alpha^{pcc} \\ V_\beta^{pcc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a^{pcc} \\ V_b^{pcc} \\ V_c^{pcc} \end{bmatrix} \quad (2)$$

To transform the alpha-beta quantities of three-phase signal into dq-rotating frame, which comprise the estimated angle (ϕ) by PLL, Park's transformation as in equation (3) is employed

$$\begin{bmatrix} V_d^{pcc} \\ V_q^{pcc} \end{bmatrix} = \begin{bmatrix} \sin(\emptyset) & -\cos(\emptyset) \\ \cos(\emptyset) & \sin(\emptyset) \end{bmatrix} \begin{bmatrix} V_\alpha^{pcc} \\ V_\beta^{pcc} \end{bmatrix} \quad (3)$$

Substituting equation (1) in equation (2), and the result of equation (2) in equation (3), thereby the equation (3) represents the transformation from three-phase to dq-synchronous rotating frame as in equation (4)

$$\begin{bmatrix} V_d^{pcc} \\ V_q^{pcc} \end{bmatrix} = \sqrt{\frac{2}{3}}|V| \begin{bmatrix} \cos(\theta - \emptyset) \\ \sin(\theta - \emptyset) \end{bmatrix} \quad (4)$$

When, the value of difference angle $(\theta - \phi)$ is small value or close to zero, $\sin(\theta - \emptyset)$ almost equal to$(\theta - \emptyset)$. During locked of PLL, the q-component of symmetrical three-phase source signals decreases to zero in synchronous coordinate system. While, q-components possesses small value due to unlocked of dq- theory based-PLL. Consequently, q-component of dq-SRF based- PLL is exploited as the detection of phase angle displacement illustrated as in Fig.2.

3.3 Proposed Disturbances Detection and Modulating Signals Determination Methods

To detect voltage disturbance and as well modulating voltage determination of three-phase individually in DVR, the dq-theory based on evaluated angle$(\emptyset)$ by utilizing a PLL are dedicated. First of all, the phase-neutral utility voltages at PCC in the pre-fault are converted into two-phase varying time as in equation (5) by Clarke's transformation, and then transformed to dq- coordinate transformation frame by Park's transformation as in equation (6)

$$\begin{bmatrix} V_\alpha^{pcc} \\ V_\beta^{pcc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a^{pcc} \\ V_b^{pcc} \\ V_c^{pcc} \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} V_d^{pcc} \\ V_q^{pcc} \end{bmatrix} = \begin{bmatrix} \sin(\emptyset) & -\cos(\emptyset) \\ \cos(\emptyset) & \sin(\emptyset) \end{bmatrix} \begin{bmatrix} V_\alpha^{pcc} \\ V_\beta^{pcc} \end{bmatrix} \quad (6)$$

As depicted in Fig. 2. An instantaneous vectors comparison is performed between the dq-quantities of phase-neutral utility voltages with the dq-quantities of reference phase-neutral utility voltages. The direct-axis reference component and quadrature-axis reference component of phase-neutral utility voltage values are put to nominal voltage value and zero respectively. When voltage disturbances occurred, the error signals appeared between the dq-quantities of utility and reference voltages. PI_d-controller and PI_q-controller are utilized for regulating these error signals of d- component and q- component independently. Consequently, these error signals are reference dq- components of DVR as in equation (7) and (8)

$$V_{d,DVR}^{ref} = V_{d,pcc}^{ref} - V_{d,pcc} \quad (7)$$

$$V_{q,DVR}^{ref} = V_{q,pcc}^{ref} - V_{q,pcc} \quad (8)$$

The outputs of the PI_d-controller and PI_q-controller converted to $\alpha\beta$- coordinate system by using inverse matrix of Park's transformation prior transmitted to MSVPWM technique.

3.4 Proposed 3-level SVPWM Technique for NPDC Converter

The 3-phase 3-level neutral point diode clamped converter illustrated in Fig. 4.a comprised three various switching states indicated as Zero, Positive, and Negative for the pole voltage. Where, positive interprets the switching statuses S_{a1+} and S_{a2+} are switched ON, thereby the (+Vdc/2) is pole voltage. Whereas the zero state of switching signifies that the switches S_{a2+} and S_{a1-} are switched ON, by that means producing a (0) voltage for pole terminal. While negative resultant and (-Vdc/2) of pole voltage means that the switches S_{a1-} and S_{a2-} are switched ON in phase leg of 3-level neutral point diode clamped converter. Fig. 4.b

demonstrates space vectors of the voltage for multi-level neutral pointe diode clamped converter.

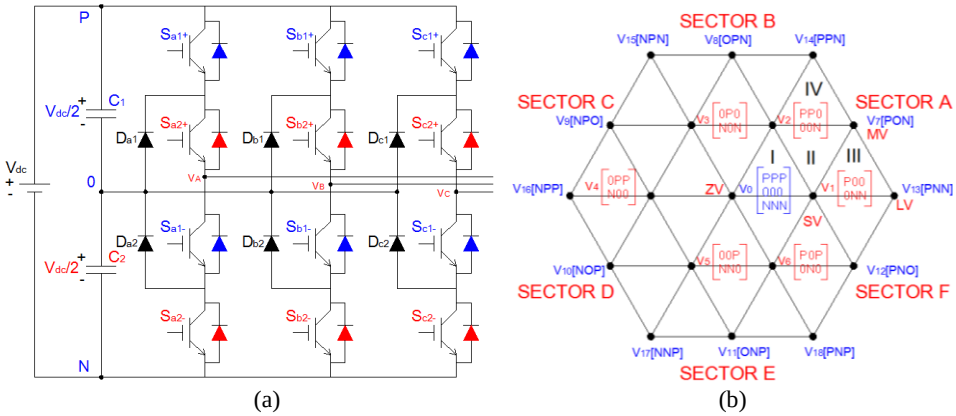


Figure 4: (a) IGBT based 3-level Neutral Point Diode Clamped Convertor. (b) Spatial vectors encompass sectors and switching states.

Each phase leg of converter comprises three statuses of switching, which produces twenty-seven vectors of voltage. These space vectors of voltage are classified to zero space vectors V0 (PPP, 000, and NNN), small space vectors V1 (0NN, P00), V2 (00N, PP0), V3(0P0, N0N), V4(0PP, N00), V5(00P, NN0), and V6(P0P, 0N0), medium space vectors V7 (P0N), V8(0PN), V9(NP0), V10(N0P), V11(0NP), and V12(PN0), and large space vectors V13(PNN), V14(PPN), through V18(PNP) as depicted in Fig. 4.b. During the switching statuses (PPP, 000, and NNN), the received power at load is zero, thereby it is indicated as zero space vector V0. The twenty-seven voltage vectors of 3-level converter are categorized to eighteen efficient voltage vectors in addition to one zero vectors as a result of analogous phase to phase of voltage level for various switching statuses, for instance (P00 and 0NN). The efficient voltage vectors comprise three levels of voltage$\left(\frac{2V_{DC}}{3}, \frac{\sqrt{3}V_{DC}}{3}, and\ \frac{V_{DC}}{3}\right)$ [23, 24, 25, and 26]. The implementation of multi-level SVPWM for 3-level NPDC inverter is achieved by utilizing the steps as follows:

3.4.1 *Identification of Sectors*

The Clarke's coordinate transformation system is dedicated to estimate the vector of reference voltage included magnitude and the angle(∅). The determination of sector rely on the reference voltage position, for angle $(0 - 60^{\circ})$ the reference voltage (V_{ref}) placed in sector A, for angle $(60^{\circ} - 120^{\circ})$ the reference voltage (V_{ref}) placed in sector B, for angle $(120^{\circ} - 180^{\circ})$ the reference voltage (V_{ref}) placed in sector C, for angle $(180^{\circ} - 240^{\circ})$ the reference voltage (V_{ref}) placed in sector D, for angle $(240^{\circ} - 300^{\circ})$ the reference voltage (V_{ref}) placed in sector E, and finally for angle$(300^{\circ} - 360^{\circ})$ the reference voltage (V_{ref}) placed in sector F.

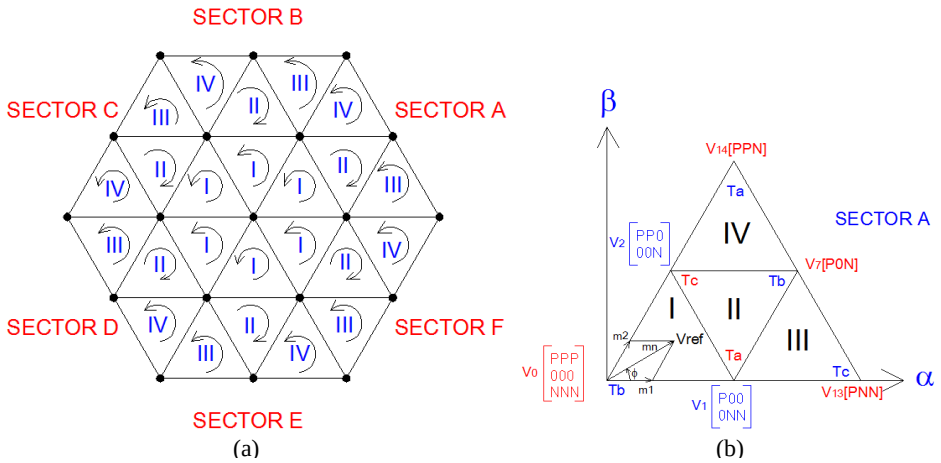


Figure 5: 3-level SVPWM. (a) Zones, sectors, and sequence of switching. (b) (m1 and m2) based (V_{ref}) staying in sector-A

3.4.2 *Identification of Zones in the Sectors*

The sector indicates to one among six triangles represented by (A, B, C, D, E, or F), as well zones with any sector are represented by I, II, III, or IV and depicted as in Fig.5.a. To identify the zones of sector where the command voltage located, m1 and m2 as clarify in Fig.5.b are calculated by utilizing equation (9) and equation (10)

$$m_1 = \frac{2}{\sqrt{3}} m_n \sin\left(\frac{\pi}{3} - \emptyset\right) \quad (9)$$

$$m_2 = \frac{2}{\sqrt{3}} m_n \sin(\emptyset) \quad (10)$$

Where, m_1 indicates the switching time of the vector-V13, m_2 indicates the switching time of the vector-V14, and $m_n = V_{ref}/\big((2/3)V_{dc}\big)$. Consequently, reference voltage (V_{ref}) located in zone-I, when m1 plus m2 equal or less than (1/2), regulating voltage (V_{ref}) stayed in zone-III when m1 greater than (1/2), command voltage (V_{ref}) placed in zone-IV when m2 greater than (1/2), and modulating voltage (V_{ref}) lying in zone-II otherwise.

3.4.3 *Estimating the Time Duration of Ta, Tb, and Tc*

To calculate the switching times of various zones (I, II, III, or IV) according to adjacent vectors strategy, the aggregate of voltages product by the time interval of selected vectors identical the multiplying of the command voltage (V_{ref}) and sampling time(T_s). For instance, if command voltage (V_{ref}) is placed in zone-II of sector A. consequently, the closest vectors to command voltage are (V_1, V_7, and V_2), thereby the equations (11-12) is employed to determine the time period $(T_a, T_b, and\ T_c)$ of voltage vectors $(V_1,\ V_7,\ and\ V_2)$ respectively.

$$V_1 T_a + V_7 T_b + V_2 T_c = V_{ref} T_s \quad (11)$$

$$T_a + T_b + T_c = T_s \quad (12)$$

Table 1 represents the duty ratios $(T_a, T_b, and\ T_c)$ of different space voltage vectors in zones (I, II, III, and IV) with sector-A.

Table 1: Duty ratios calculation in zones with sector-A for modulation voltage

Zones	Duty Ratios		
	T_a	T_b	T_c
I	$T_s\left[2Mn * \sin\left(\frac{\pi}{3}-\emptyset\right)\right]$	$T_s\left[1-2Mn * sin\left(\frac{\pi}{3}+\emptyset\right)\right]$	$T_s[2Mn * \sin(\emptyset)]$
II	$T_s[1-2Mn * \sin(\emptyset)]$	$T_s\left[2Mn * \sin\left(\frac{\pi}{3}+\emptyset\right)-1\right]$	$T_s\left[1-2Mn * \sin\left(\frac{\pi}{3}-\emptyset\right)\right]$
III	$T_s\left[2-2Mn * \sin\left(\frac{\pi}{3}+\emptyset\right)\right]$	$T_s[2Mn * \sin(\emptyset)]$	$T_s\left[2Mn * \sin\left(\frac{\pi}{3}-\emptyset\right)-1\right]$
IV	$T_s[2Mn * \sin(\emptyset)-1]$	$T_s\left[2Mn * \sin\left(\frac{\pi}{3}-\emptyset\right)\right]$	$T_s\left[2-2Mn * \sin\left(\frac{\pi}{3}+\emptyset\right)\right]$

3.4.4 *Determining the Switching Sequence*

As illustrated in Fig.5.a. The sequence of switching is achieved for each zone (I, through IV) in sectors (A, to F) by taking into account, one switch operated at same time. Thereby, switching orders for each zone (I, to IV) in sector-A are specified as below.

Zone- I (13-segments): -1-1-1(V0),0-1-1(V1),00-1(V2),000(V0),100(V1),110(V2),111(V0), 110 (V2),100(V1),000 (V0),00-1 (V2),0-1-1 (V1),-1-1-1 (V0).
Zone- II (9-segments): 0-1-1(V1),00-1(V2),10-1(V7),100(V1),110(V2),100(V1),10-1(V7), 00-1(V2),0-1-1 (V1).
Zone- III (7-segments):0-1-1(V1),1-1-1(V13),10-1(V7),100(V1),10-1(V7),1-1-1(V13),0-1-1(V1).
Zone- IV (7-segments):00-1(V2),10-1(V7),11-1(V14),110(V2),11-1(V14),10-1(V7),00-1(V2).

Consequently, switching sequence of sector-A in zones (I, II, III, and IV) for reference voltage are demonstrated in Fig. 6.

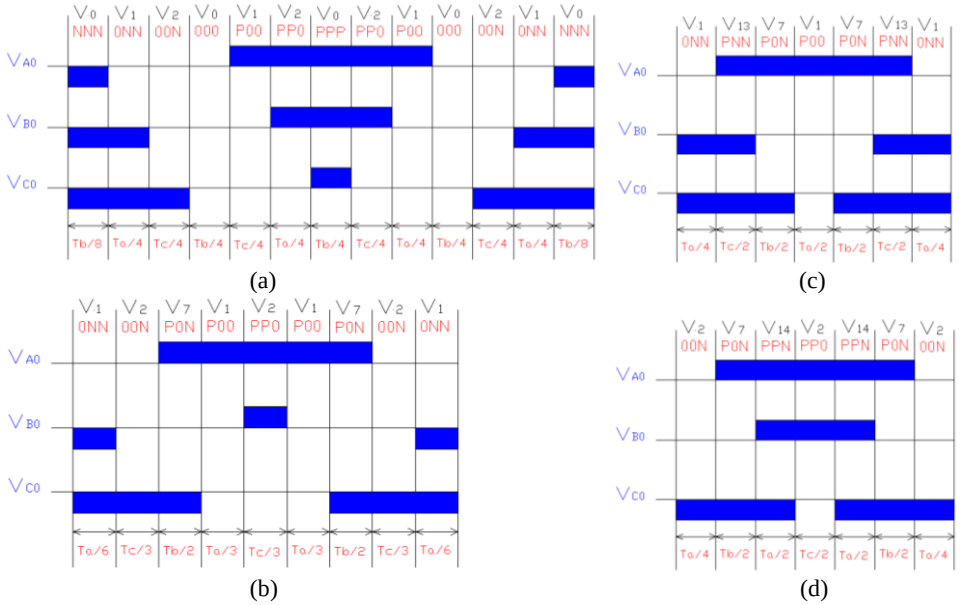


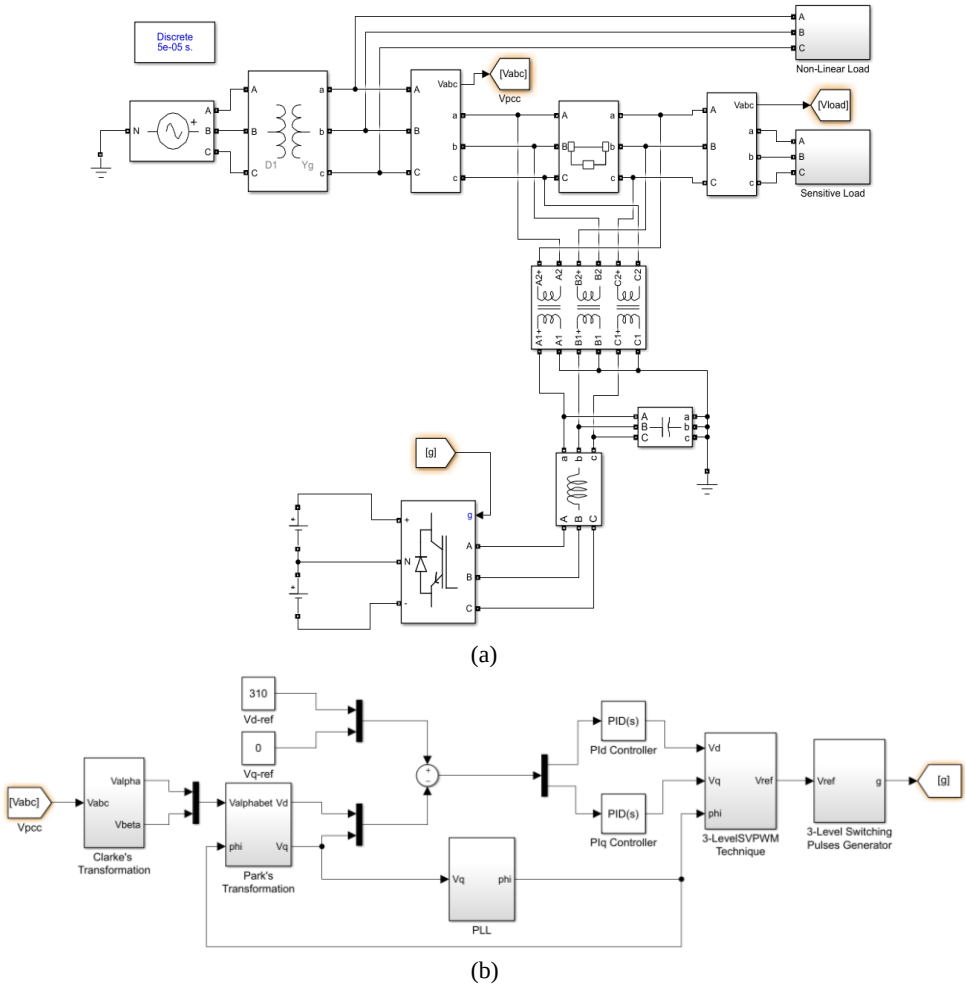
Figure 6: Sequence signals of command voltage switching with sector-A. (a) Zone (I). (b) Zone (II). (c) Zone (III). (d) Zone (IV).

4. SIMULATION RESULTS AND DISCUSSION

To verify the effectiveness of the proposed control strategy under various disturbance conditions of voltage source, a simulation model of multi-level space vector PWM technique based- dynamic voltage restorer as exhibited in Fig. 7 with parameters listed in Table 2 is performed by employed the power system environment of MATLAB/SIMULINK program.

Table 2: Parameters Dedicated for Simulation Model of Presented Work

Parameter	**Value/Electronic Devices**
Line Voltage	380 V, 50 Hz
Injection Transformer Ratio	1:2
Non-linear Load	3- phase Controlled Thyristor-Rectifier Fed (200 Ω and 80 mH)
DC-bus Voltage/Battery	200 V
Harmonic Filter	6 mH and 20 μF
Frequency of SVPWM Switching	950 Hz
VSI	IGBT/Diodes



(a)

(b)

Figure 7: Simulation model of 3-Level SVPWM based- DVR. (a) Power network. (b) Control strategy.

4.1 Results of simulation model under balanced distortion voltage

4.1.1 Without injected voltage by DVR

The distortion in source voltage created by non-linear load comprised three-phase controlled thyristor-rectifier fed impedance load connected to PCC reflected in load voltage in which the load voltage (Fig.8.c) is identical as the source voltage (Fig.8.a). The real (red) and reactive (blue) powers delivered to the load (Fig.8.f) without injected voltage and power (Fig.8.b and Fig.8.e) respectively by DVR is same as the supply power (Fig.8.d).

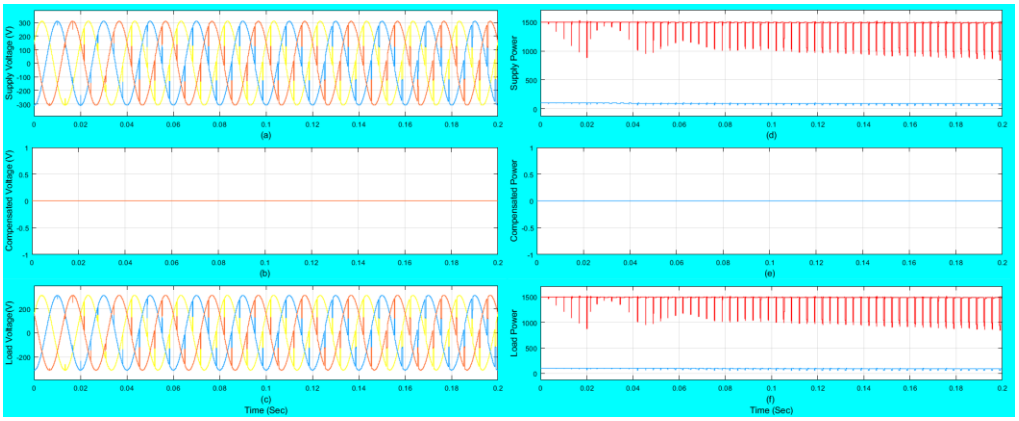


Figure 8: Without injected voltage by DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

4.1.2 With Injected Voltage by 2-level SVPWM Based- DVR

The 2-level SVPWM based- DVR respond to distortion supply voltage (Fig.9.a) and injects the compensating voltage (Fig.9.b). After distortion voltage compensation, the load voltage (Fig.9.c) regains its previous profile. To mitigate the harmonics in source voltage, 2-level SVPWM based- DVR is supplied the required in active and reactive powers to load (Fig.9.e) and maintains the load power (Fig.9.f) at nominal value.

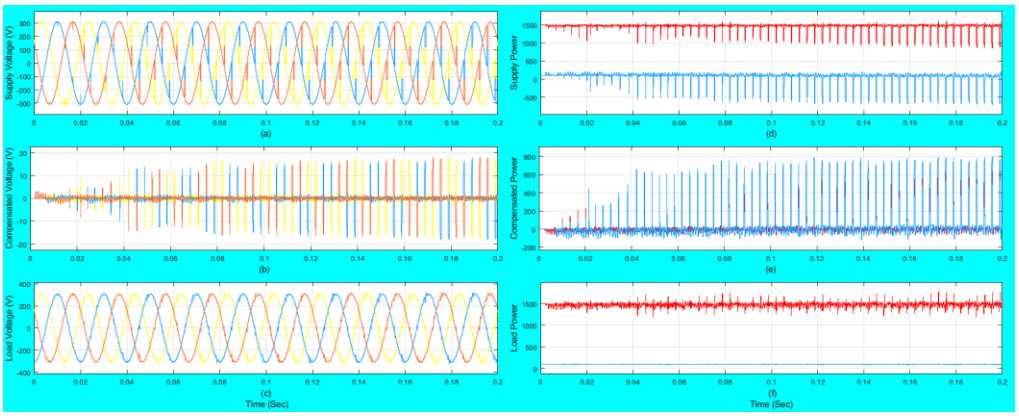


Figure 9: With injected voltage by 2-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

4.1.3 With Injected Voltage by 3-level SVPWM Based- DVR

The compensation voltage by 3-level SVPWM based- DVR evident by Fig.10.b. The voltage at load (Fig.10.c) after compensation by 3-level SVPWM based- DVR are ideal sinusoidal and comprise very small ripple compared to 2-level SVPWM based- DVR (Fig.9.c). The injected power by 3-level SVPWM based- DVR illustrated in Fig.10.e, by means of that reduction of ripple at load power (Fig.10.f) ascertained by using 3-level SVPWM based- DVR in comparison with 2-level SVPWM based- DVR (Fig.9.f).

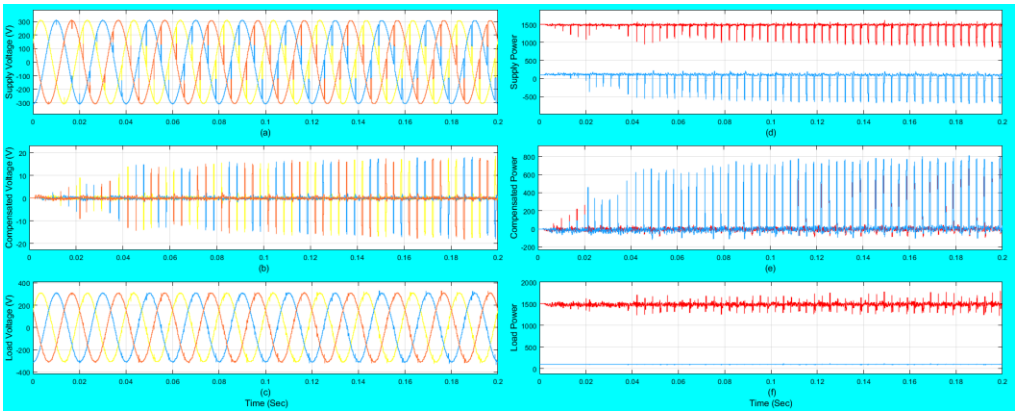


Figure 10: With injected voltage by 3-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

Fast Fourier Transform as illustrated in Fig.11 exploited to analysis the voltages of sensitive load without and with various compensation voltages by DVR. The load voltage with employed 3-level SVPWM based-DVR attained a considerable mitigation in 2.02% THD as demonstrated in Fig.11.c in comparison to 15.39% THD without compensated voltage by DVR as depicted by Fig.11.a and higher efficiency than 3.37% THD when applied 2-level SVPWM based- DVR as exhibited in Fig.11.b.

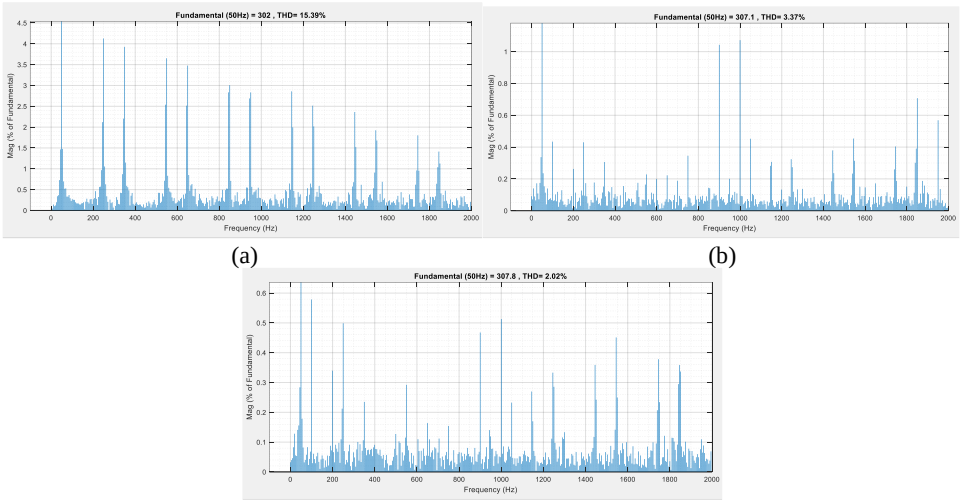


Figure 11: Spectrum of FFT with THD% for load voltage. (a) Without injected voltage DVR. (b) With injected voltage by 2-level SVPWM based- DVR. (c) With injected voltage by 3-level SVPWM based-DVR.

4.2 Results of Simulation Model under Balanced Distortion Voltage Disturbances

4.2.1 Balanced distortion voltage sag

The balanced distortion voltage sag with a depth of 50% voltage of its nominal value produced by using programmable block of voltage supply from 60 to 140 msec. The 2-level SVPWM based- DVR injects required voltage (Fig.12.b) in phase with respect to voltage of supply (Fig.12.a) to maintain load voltage (Fig.12.c) at nominal value. During sag period, 2-level SVPWM based- DVR supplied the decrease in real (red) and reactive (blue) powers (Fig.12.e) to load, thereby maintain the load power (Fig.12.f) at nominal value.

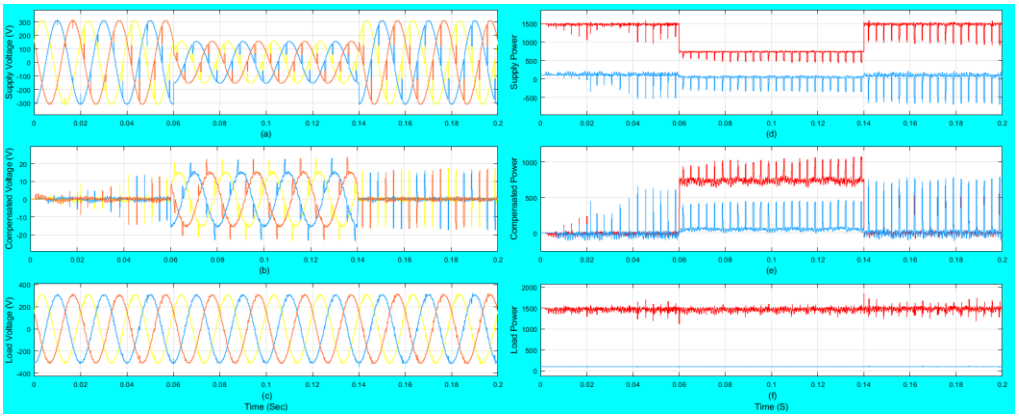


Figure 12: Compensation of balanced voltage sags by 2-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

Proposed 3-level SVPWM technique based- DVR under balanced distortion voltage sag effectively responded to voltage sag as demonstrated in Fig.13, load voltage waveform (Fig.13.c) with 3-level SVPWM are ideal in addition to provide real and imaginary power to load (Fig.13.f) accompanied with less ripple compared to 2-level SVPWM method based-DVR (Fig.12.c and Fig.12.f) respectively.

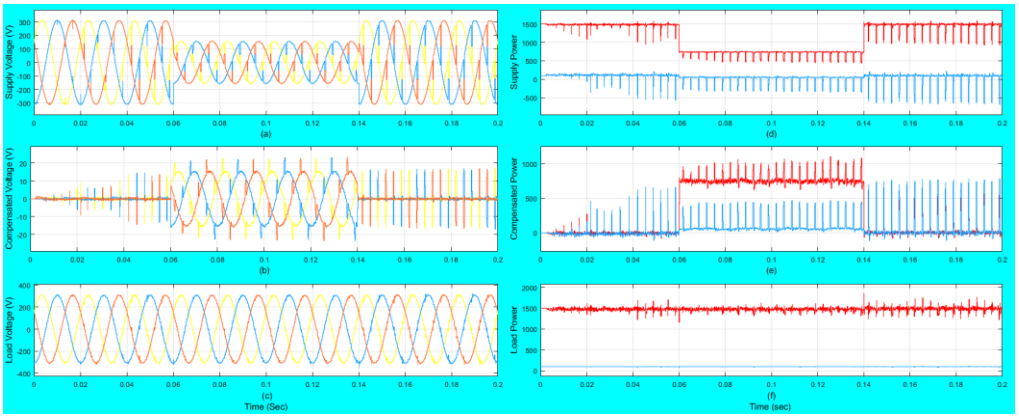


Figure 13: Compensation of balanced distortion voltage sag by 3-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

4.2.2 Balanced Distortion Voltage Swell

The balanced distortion voltage swell with a rise of 150% voltage of its nominal value is created by using programmable block of voltage supply from 60 to 140 msec. 2-level SVPWM based- DVR injects required voltage (Fig.14.b) in phase opposition with respect to voltage of supply (Fig.14.a) to preserve the nominal voltage at load (Fig.14.c). During swell interval, 2-level SVPWM based- DVR is absorbed the increase in active (red) and reactive (blue) powers (Fig.14.e) to load; by that means maintain the load power (Fig.14.f) at nominal value.

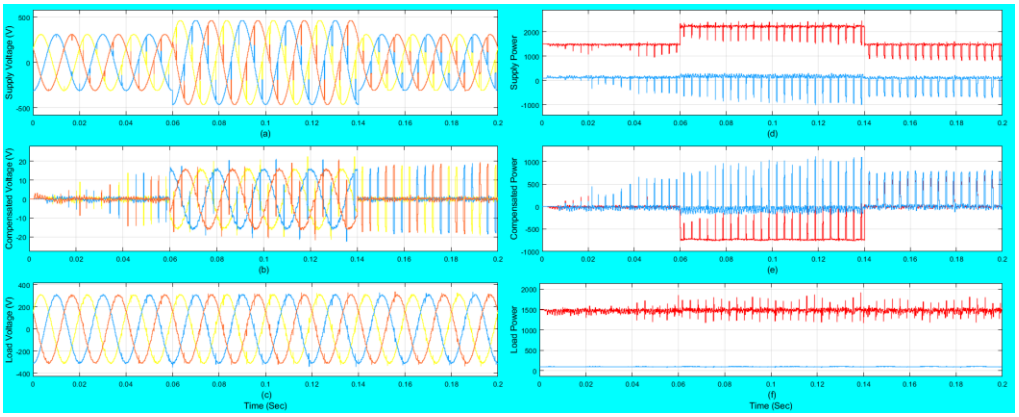


Figure 14: Compensation of balanced distortion voltage swells by 2-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

Results of simulation model with utilized 3-level SVPWM technique based- DVR under balanced distortion voltage swell as illustrated in Fig.15. Waveforms of load voltage (Fig.15.c) are more sinusoidal extra to supply real and reactive power to load (Fig.15.f) is lower ripple compared to 2-level SVPWM technique based-DVR (Fig.14.c and Fig.14.f) respectively.

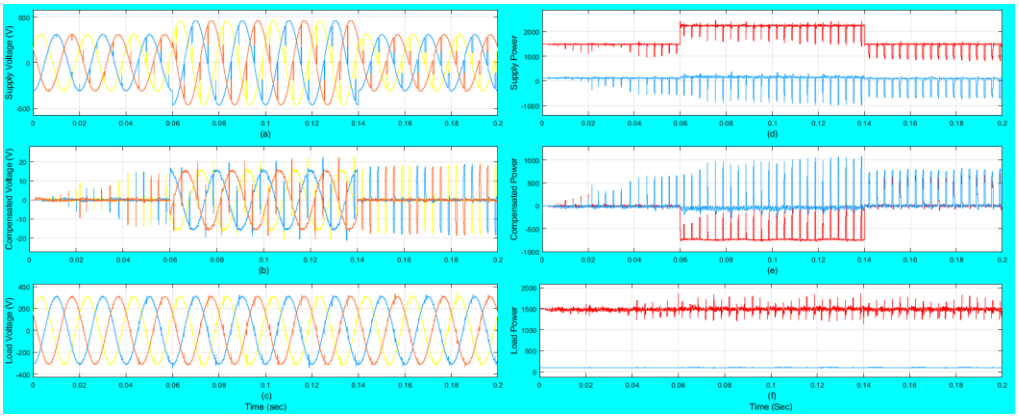


Figure 15: Compensation of balanced distortion voltage swells by 3-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

Spectrum of FFT with THD% for load voltages under balanced distortion voltage source sag and swell utilized 2-level SVPWM based- DVR and 3-level SVPWM based- DVR respectively are demonstrated in Fig.16. Significant mitigation with 3-level SVPWM based-DVR (1.77% and 2.14%) achieved as illustrated in (Fig16.b and Fig16.d) in comparison to 2-level SVPWM based- DVR (3.04% and 3.84%) as demonstrated in (Fig16.a and Fig16.c) in THD under balanced distortion voltage sag and swell respectively.

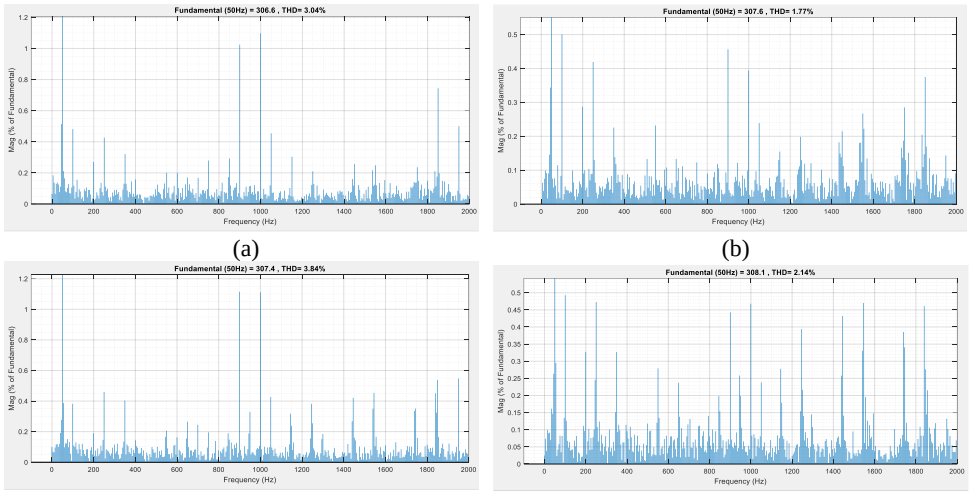


Figure 16: Spectrums of FFT with THD% for load voltage. (a) 2-level SVPWM based- DVR under balanced voltage sag. (b) 3-level SVPWM based- DVR under balanced voltage sag. (c) 2-level SVPWM based- DVR under balanced voltage swell. (d) 3-level SVPWM based- DVR under balanced voltage swell.

4.3 Results of Simulation Model under Unbalanced Distortion Voltage Disturbances

4.3.1 Unbalanced distortion voltage sag

The unbalanced distortion voltage sag with different depth of phase voltage of its nominal voltage is created by using programmable block of voltage supply from 60 to 140 msec. The 2-level SVPWM based- DVR injects the appreciated voltage (Fig.17.b) in individual phase to retain the nominal voltage at load (Fig.17.c). During unbalanced voltage sag period (Fig.17.a), 2-level SVPWM based- DVR supplied (Fig.17.e) the decrease in active (red) and reactive (blue) powers to load and maintains the load power (Fig.17.f) at nominal value.

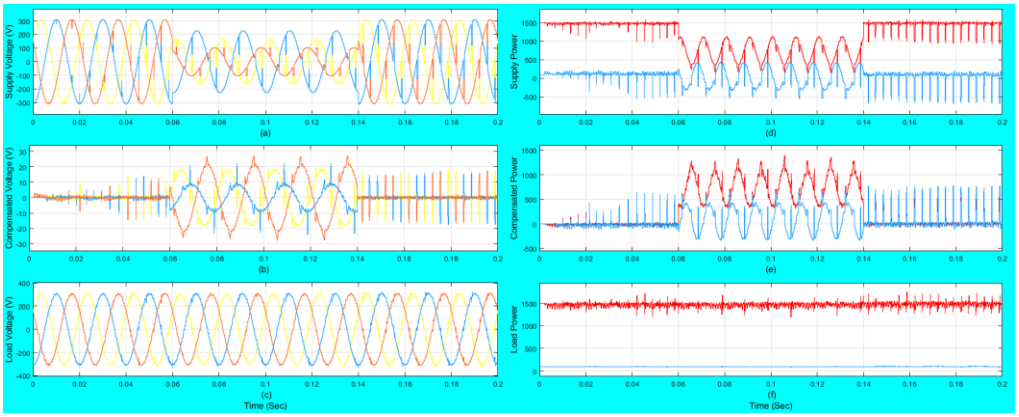


Figure 17: Compensation of unbalanced distortion voltage sag by 2-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

Figure 18 shows the simulation results under unbalanced distortion voltage sag employed 3-level SVPWM based- DVR. As obvious in (Fig.18.c and Fig.18.f) compared to 2-level

SVPWM (Fig.17.c and Fig.17.f) respectively, the voltage waveforms are smoother and powers (active and imaginary) accompanied with tiny ripple at load.

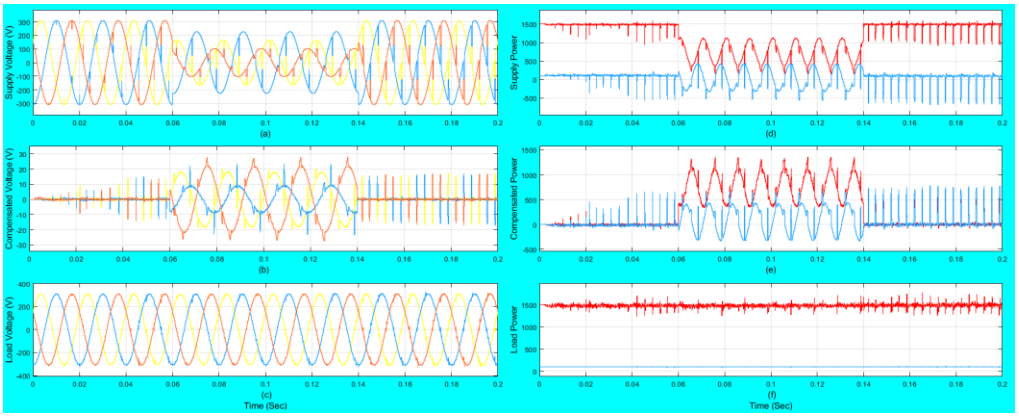


Figure 18: Compensation of unbalanced distortion voltage sag by 3-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

4.3.2 Unbalanced Distortion Voltage Swell

The unbalanced distortion voltage swell with different rise of phase voltage of its nominal voltage in Fig.19.a is created by using programmable block of voltage supply from 60 to 140 msec. The 2-level SVPWM based- DVR injects the required voltage in individual phases in phase opposition (Fig.19.b) to maintain the nominal load voltage (Fig.19.c). During unbalanced distortion voltage swell period, 2-level SVPWM based- DVR is absorbed the increase (Fig.19.e) in active (red) and reactive (blue) powers to load and maintains the load power (Fig.19.f) at nominal value.

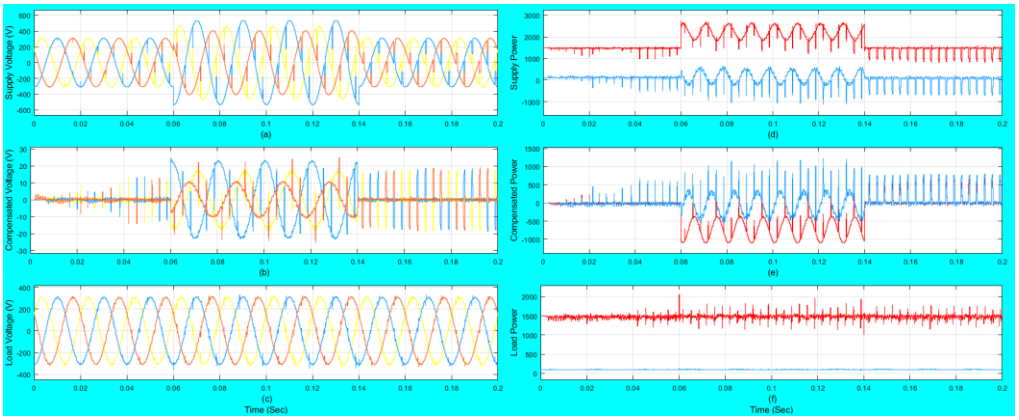


Figure 19: Compensation of unbalanced distortion voltage swell by 3-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

Fig.20 depicts optimize responded of 3-level SVPWM based- DVR exploited as compensation of distortion voltage swell under unbalanced condition. During unbalanced distortion voltage swell interval, ideal sinusoidal load voltage (Fig.20.c) and lower ripple at load power (Fig.20.f) are achieved compared to 2-level SVPWM based DVR (Fig.19.c and Fig.19.f) respectively.

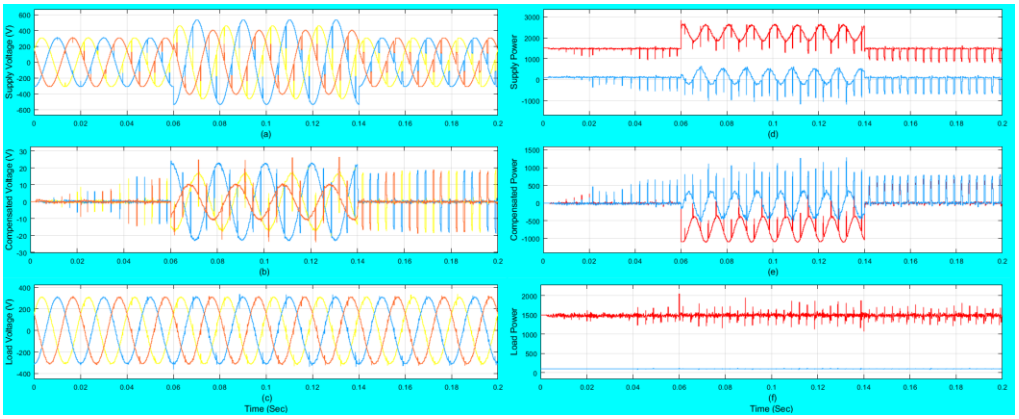


Figure 20: Compensation of unbalanced distortion voltage swell by 3-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

4.3.3 Unbalanced Distortion Voltage Disturbance Compiles Sag and Swell.

The unbalanced distortion voltage sag/swell with different dip/rise of phase voltage of its nominal voltage is created (Fig.21.a) by using programmable block of voltage supply from 60 to 140 msec. The 2-level SVPWM based- DVR injected/absorbed the required voltage in individual phases in phase/opposition (Fig.21.b) with respect to source voltage to maintain the nominal voltage at load (Fig.21.c). During unbalanced voltage sag/swell period, 2-level SVPWM based- DVR supplied/absorbed the decrease/increase in real (red) and imaginary (blue) powers (Fig.21.e), thereby maintains the load power at nominal value (Fig.21.f).

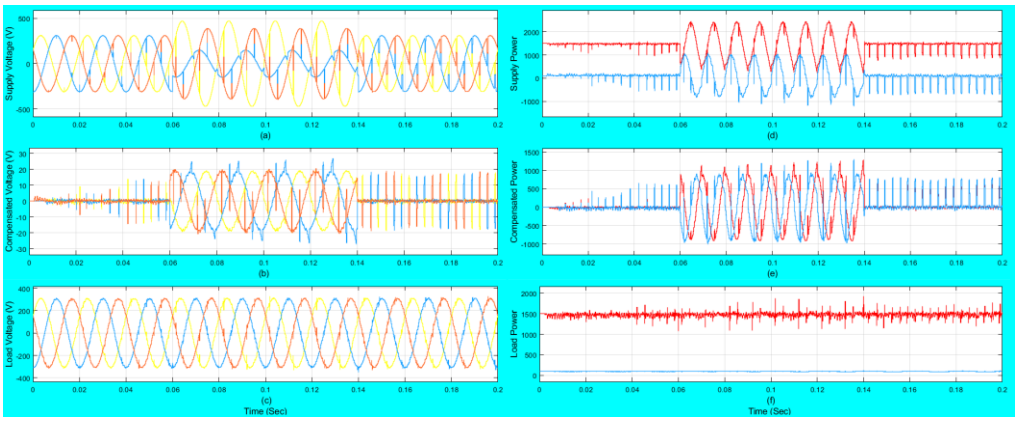


Figure 21: Compensation of unbalanced distortion voltage sag/swell by 2-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

Presented unbalanced distortion voltage disturbance comprised sag and swell are compensated perfectly by dedicated 3-level SVPWM based-DVR as illustrated in Fig.22. In comparison with 2-level based- DVR (Fig.21.c and Fig.21.f), ideal sinusoidal voltage waveform and tiny ripple of power are attained by 3-level based- DVR (Fig.22.c and Fig.22.f) respectively at sensitive load.

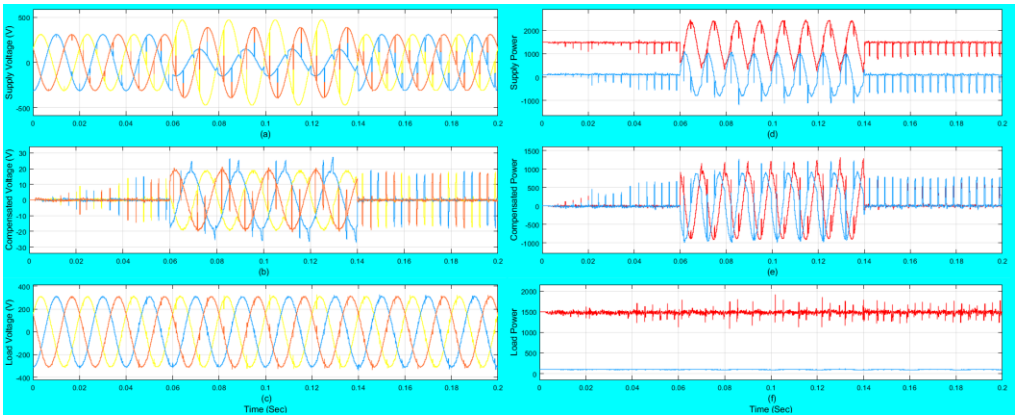


Figure 22: Compensation of unbalanced distortion voltage sag/swell by 3-level SVPWM based-DVR. (a) Voltage at PCC. (b) Compensated voltage. (c) Voltage at load. (d) Supply power. (e) Compensated power. (f) Load power.

Spectrums of FFT with THD% for load voltage under unbalanced distortion voltage sag, voltage swell and voltage sag/swell applied 2-level SVPWM based- DVR and 3-level SVPWM based- DVR respectively are demonstrated in Fig. 23. Significant mitigation with 3-level SVPWM based- DVR (Fig.23.b, Fig.23.d, and Fig.23.f) attained in comparison to 2-level SVPWM based- DVR (Fig.23.a, Fig.23.c, and Fig.23.e) in THD% under unbalanced distortion voltage sag, swell and sag/swell respectively as tabulated in table 3.

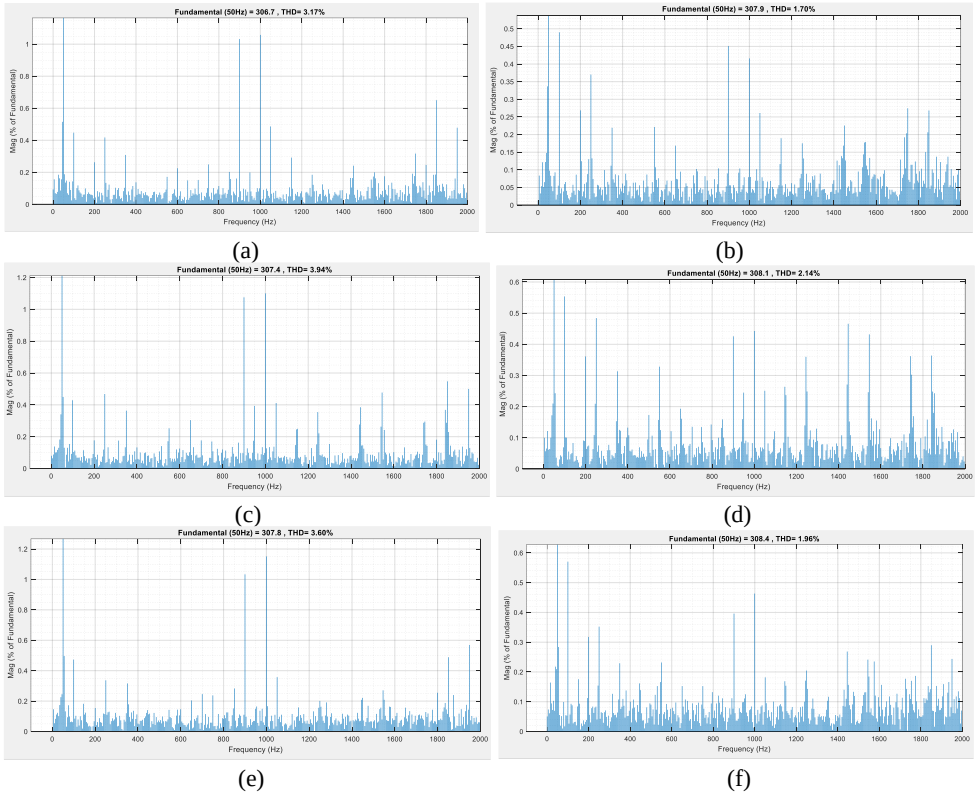


Figure 23: Spectrums of FFT with THD% for load voltage. (a) 2-level SVPWM based- DVR under unbalanced voltage sag. (b) 3-level SVPWM based- DVR under unbalanced voltage sag. (c) 2-level SVPWM based- DVR under unbalanced voltage swell. (d) 3-level SVPWM based- DVR under

unbalanced voltage swell. (e) 2-level SVPWM based- DVR under imbalanced voltage compiles sag and swell. (f) 3-level SVPWM based- DVR under imbalanced voltage compiles sag and swell.

Table 3: Comparative load voltage analysis of THD% under various disturbances

Voltages at PCC	Disturbances	2-level SVPWM-DVR	3-level SVPWM-DVR
Balanced distortion	-	3.37%	2.02%
Balanced distortion	Sag	3.04%	1.77%
	Swell	3.84%	2.14%
Unbalanced distortion	Sag	3.17%	1.70%
	Swell	3.94%	2.14%
	Sag/Swell	3.60%	1.96%

5. CONCLUSION

In this work, the effectiveness of a 3-level SVPWM based- neutral point diode clamped converter employed low frequency as triggering pulses with series voltage regulator (SVR) well renowned as dynamic voltage restorer in alleviating voltage sags/swells and mitigation of harmonics under balanced and imbalanced distribution network voltage conditions are attained by dedicated software package environment of MATLAB/SIMULINK. A pre-disturbance strategy for voltage compensation and the phase-locked-loop based dq-synchronous coordinate transformation are proposed as a control strategy which is exhibited superior performance with rapid dynamic response to restorer the profile of load voltages during various disturbance conditions. With proposed model, when simulation under balanced distortion voltage, the load voltage with applied 3-level SVPWM based- DVR achieved a significant mitigation in 2.02% of THD in comparison to 15.39% THD without injected voltage by DVR, and higher efficiency than 3.37% of THD when employed 2-level SVPWM based- DVR. Whereas under balanced distortion voltage sag and swell respectively, considerable reduction with 3-level SVPWM based-DVR (1.77% and 2.14%) attained in comparison to 2-level SVPWM based- DVR (3.04% and 3.84%) of THD. While under unbalanced distortion voltage sag, swell, and sag/swell respectively, significant mitigation with 3-level SVPWM based-DVR (1.70% , 2.14% , and 1.96%) achieved in comparison to 2-level SVPWM based-DVR (3.17% , 3.94% , and 3.60%) of THD. Further mitigation of load voltages (THD%) achieved and within 5% as limited by IEEE- harmonics standard 519-1992 [27] as illustrated in table 3 by utilized the spectrum analysis of FFT . Simulation results revealed the efficiency of the presented work to eliminate the harmonic distortion and to inject the desired quantities of voltage under symmetrical and unsymmetrical conditions to maintain the voltage waveform of loads ideally at rated magnitude and frequency. Moreover, balances the variation of real and imaginary power with least ripple are effectively accomplished with the presented model of DVR.

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