HALF BRIDGE RESONANT INVERTER

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ABSTRUCT
The aim of this work is to develop a resonant inverter using half bridge inverter configuration which feed power to induction heater during positive and negative cycle of load current. Such system will substitute the using of full bridge configuration, hence a reduction in both cost and complexity. A full analysis of the proposed circuit using IGBTs at a frequency of 50 kHz, and a power of 1.8 kW is presented. The practical results agree with that of the simulation, and their waveforms are closely similar, so the proposed inverter is completely valid.

KEYWORDS: Bridge transistor, gate drive, Induction heating, Orcad, Resonant inverter.

عاكس رنين نصف القنطرة

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المستخلص
الهدف من هذا العمل هو تطوير عاكس رنين بواسطة استعمال عاكس نصف قنطرة قادر على تجهيز القدرة إلى فرن حثي خلال كل من نصف الدورة الموجب والسالب للتيار. إن هذا العمل سوف يستعيض عن استخدام قنطرة كاملة مما يؤدي إلى تخفيض كل من الكلفة وتعقيد الدائرة. تم في هذا العمل إعطاء تحليل كامل للدائرة المقترحة باستخدام ترانزستورات نوع IGBTs بتردد ٥٠ كيلو هرتز وبقدرة مقدارها ١,٨ كيلو وات. وقد تطابقت النتائج الممثلة مع النتائج العملية مما يثبت فاعلية الدائرة المقترحة.

INTRODUCTION
To feed power to the load during both positive and negative cycles of load current, a full bridge inverter is used as in [3], and the soft switching of such system is explained in [1], but in the conventional half bridge resonant inverter shown in **fig. 1** the power is fed to the load only during the period when T1 is turned on. The suggested design **fig. 2** feed power to load during both periods of operation of T1 and T2. The value of the capacitors (C1 & C2) is half the value of (C) used in **fig.1**, but two capacitors are needed so their sum is the same of that used in conventional approach. These capacitors should be from same type and manufacturer so that their effective series resistance is the same.

OPERATION MODES
Mode 1
This mode is shown in **fig. 3**, where T1 is closed and T2 is open.

Mode 2

This mode is shown in **fig. 4**, where T1 is open and D2 is closed

Mode 3

This mode is shown in **fig. 5**, where T1 is open and T2 is closed.

Mode 4

This mode is shown in **fig. 6**, where D1 is closed and T2 is open.

RESONANCE FREQUENCY

In the four modes of operation **figures (3-6)** the equivalent circuit consists of parallel impedance (C, R&L) in series with capacitive impedance (C): in modes (1&2) the currents (i_{C1}, i_{C2}, and i_L) are as indicated in the figures (3&4), so the source voltage is applied in the positive direction. In modes (3&4) all the currents (i_{C1}, i_{C2}, and i_L) are reveres and hence the source voltage is applied in the negative direction. Hence the equivalent circuit can be represented by using a square-wave voltage source, parallel impedance, and series impedance as shown in **fig. 7**.

The Laplace transform of the source voltage (V_S) is as in eq (1) below: [2]

$$\mathcal{L}[V_S] = \frac{V}{S}\,\frac{1-2e^{\frac{-ST}{2}}-e^{-ST}}{1-e^{-ST}} \tag{1}$$

Now from fig. 7 the parallel impedance Z_P is:

$$Z_P = Z_C \mathbin{/\!/} Z_L \tag{2}$$

Where Z_C is the capacitor impedance ($\frac{1}{SC}$), Z_L is the load impedance (R+SL).

The total impedance Z_t is:

$$Z_t = Z_P + Z_C \tag{3}$$

The voltage across the parallel branch (V_P) is:

$$V_P = V_S\,\frac{Z_P}{Z_P+Z_C} \tag{4}$$

$$\therefore\ V_P = V_S\,\frac{Z_P}{Z_t} \tag{5}$$

The load current is $I_L = \frac{VP}{Z_L}$ (6)

$$Z_P = \frac{\frac{1}{SC}(SL+R)}{\frac{1}{SC}+(SL+R)}$$

$$\therefore Z_P = \frac{SL+R}{S^2LC+SRC+1} \tag{7}$$

$$Z_t = \frac{SL+R}{S^2LC+SRC+1}+\frac{1}{SC}$$

By simplifying $Z_t = \frac{2S^2LC+2RC+1}{(SC)(S^2+SRC+1)}$ (8)

Substituting eq.s (1), (7) and (8) in (5) to get:

$$V_P = \frac{V}{S}\,\frac{1-2e^{\frac{-ST}{2}}-e^{-ST}}{1-e^{-ST}}\,\frac{\frac{SL+R}{S^2LC+SRC+1}}{\frac{2S^2LC+2SRC+1}{(SC)(S^2LC+SRC+1)}}$$ and by simplifying:

$$V_p=\frac{V}{S}\,\frac{1-2e^{\frac{-ST}{2}}-e^{-ST}}{1-e^{-ST}}\,\frac{(SC)(SL+R)}{2S^2LC+2SRC+1} \tag{9}$$

Substituting (9) in (6):

$$I_L=\frac{\frac{V}{S}\,\frac{1-2e^{\frac{-ST}{2}}-e^{-ST}}{1-e^{-ST}}\,\frac{(SC)(SL+R)}{(2S^2LC+2SRC+1)}}{(SL+R)} \tag{10}$$

After simplifying:

$$I_L=\frac{V}{\omega_0 L}\left[\frac{\frac{1}{2}}{1-e^{-ST}}\,\frac{\omega_0}{\left(S+\frac{1}{2}\frac{R}{L}\right)^2+\omega_0^2}-\frac{e^{-\frac{ST}{2}}}{1-e^{-ST}}\,\frac{\omega_0}{\left(S+\frac{1}{2}\frac{R}{L}\right)^2+\omega_0^2}+\frac{\frac{1}{2}e^{-ST}}{1-e^{-ST}}\,\frac{\omega_0}{\left(S+\frac{1}{2}\frac{R}{L}\right)^2+\omega_0^2}\right] \tag{11}$$

Hence it can be obtained that I_L is a periodic function and its function for one half cycle is:

$$I_L(t)=\frac{V}{\omega_0 L}e^{-\frac{R}{2L}t}\left(\frac{1}{2}\sin\omega_o t-\sin\left(\omega_o t+\frac{T}{2}\right)+\frac{1}{2}\sin\left(\omega_o t+T\right)\right) \tag{12}$$

Where:

$$\omega_0=\sqrt{\frac{1}{2LC}-\frac{1}{4}\left(\frac{R}{L}\right)^2} \tag{13}$$

$$\therefore \text{the resonance frequency is}\quad f_0=\frac{1}{2\pi}\sqrt{\frac{1}{2LC}-\frac{1}{4}\left(\frac{R}{L}\right)^2} \tag{14}$$

$$\text{Where } T=\frac{1}{f_0} \tag{15}$$

In this work V = 50V, R = 0.5 ohm, L = 5μH, C = 1μF, so f_O can be calculated from eq. (14), hence f_O = 49.7 kHz.
The maximum current I_{Lmax} occurred at $\omega_o t = (\pi/2)$ or (t=T/4 = 5μs) and can be calculated from eq. (12),

$$I_L=\frac{50}{2\pi*49.7*10^3*5*10^{-6}}\,e^{-\frac{0.5*5\mu}{2*5\mu}}\left\{\frac{1}{2}-(-1)+\frac{1}{2}\right\}=49.96A$$

DRIVING CIRCUIT

If the output impedance of the gate drive circuit is high, the change of collector-emitter voltage at high frequencies will be reflected to the gate circuit, causing permanent damage. [4]. So in this work a low output impedance driving circuit is used, that is not only gate-emitter voltage rating not exceeded, but also the voltage transient at the gate is contained to a level at which spurious turn-on not occurred. This driving circuit is IR2110 (International Rectifier Control IC).
But this driving circuit control IC suffers from:

i. Low output current.
ii. It have a share common for both input and output

The problem (i) solved by using a power amplification buffer between the control IC and the gate-emitter, [5].
The problem (ii) solved by inserting a resistance between the common and the low side emitter [6].

SIMULATION

The simulation is implemented using Orcad 16.2 software. The circuit used in this simulation is show in **fig. 8**.

Fig. 9 shows the waveforms of load current and collector-emitter voltage. The current waveform is sinusoidal of peak value of 52 A which is very near to the calculated theoretical value (49.96 A). Also it is obvious that the current is switched at zero voltage (resonance). Also it is obvious that the frequency is 50 kHz equal with calculated value.

Fig. 10 shows the waveforms of load current and load voltage. The waveform of the load voltage is not strange, it is expected to be like this because in mode 1& 4 (**fig. 3&6**) the load voltage is the voltage of capacitor C1, and in modes 2&3 (**fig. 4&5**) the load voltage is the voltage of capacitor C2, so the switching between these modes is the reason of the step change in the load voltage, however this change is not sever as it shown equal about to 40V,and still the load current waveform is a sine wave.

In **fig. 11** the voltage waveforms of the capacitors C1 & C2 are shown. The waveforms are pure sinusoidal, so in each time of the four modes (3-6), a pure sine voltage is applied across the load.

PRACTICAL RESULT

In **fig.12** the gate signal waveforms are shown, the dead time is 1µs, the frequency is 50 kHz. Voltage scale is 5V/Div, Time scale is 5µs/Div.

In **fig. 13** the voltage waveforms of load current and transistor collector-emitter voltage are shown. The current is pure sine wave, and the switching is in the zero current crossing. The practical result is completely same as the simulated result (fig. 9), but the waveforms in the simulation is in the same scale, but practically is not. Voltage scale is 20 v/Div; Current Scale is 15A/Div, Time scale 5µs/Div

In **fig. 14** the load voltage and load current are shown. The peak load current is about 47A which is very similar to the simulated and with the calculated one. The voltage scale is 20 V/Div, Current scale is 15 A/Div, Time Scale is 5µs/Div.

In **fig. 15** the voltage waveforms of both C1 and C2 are shown. The waveforms are pure sine waves and completely similar to the simulated one. Voltage scale 20V/Div, Time scale 5µs/Div.

Fig. 16 shows a part of the project.

In **fig. 17** and **fig. 18** the element heated and reached the red color at about 700°.

REFERENCES

[1] Dede, V. Esteve, E. Maset, J. M. Espf, A. E. Navaro…"soft switching series resonant converter for induction heating applications" IEEE, International Conference 1995.

[2] Katsuhiko Ogata: "Modern Control Engineering", Fourth Edition, 2002, pp 46

[3] Xiaorong Zhu, Yonglong Peng, Xinchun Shi, Heming Li, "200kW f400kHz High Frequency Inverter For Induction Heating Application", IEEE PEDS 2005.

[4] International Rectifier Application Note, AN-936, Sec 3.

[5] International Rectifier Application Note, AN-978, Sec 7.

[6] International Rectifier Design Tip, Dt97-3, Sec 8.

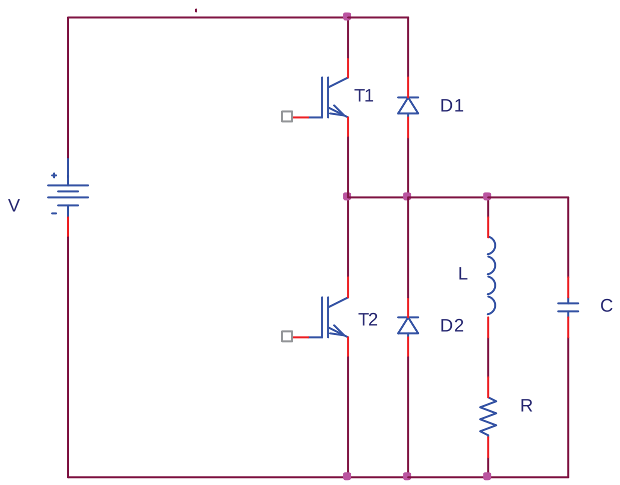


Fig. 1
Conventional half bridge inverter resonant inverter

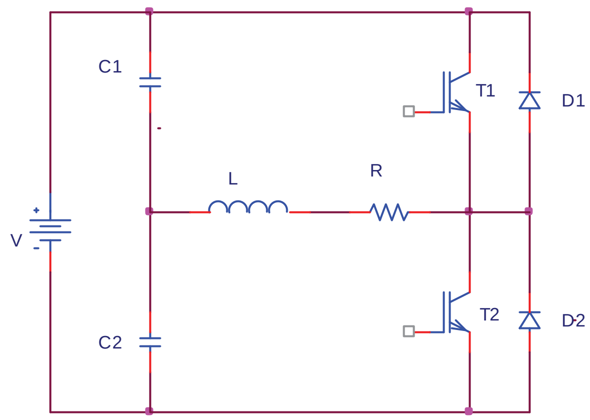


Fig. 2
Suggested design

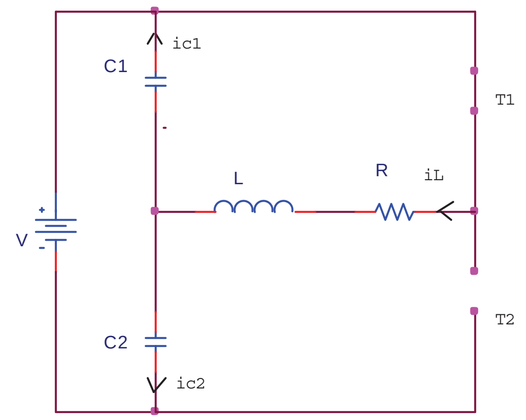


Fig. 3
(In this mode only T_1 is turned-on)

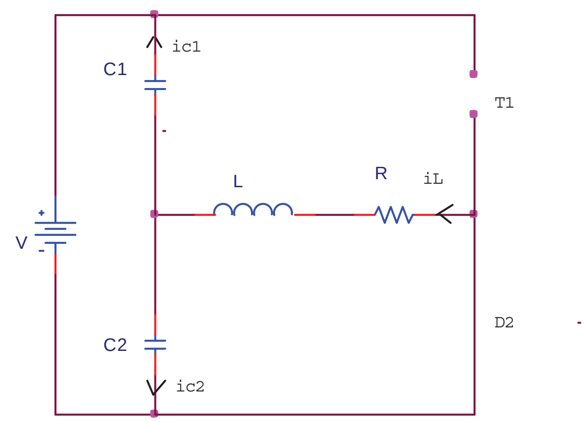


Fig. 4
(In this mode only D_2 is turned-on)

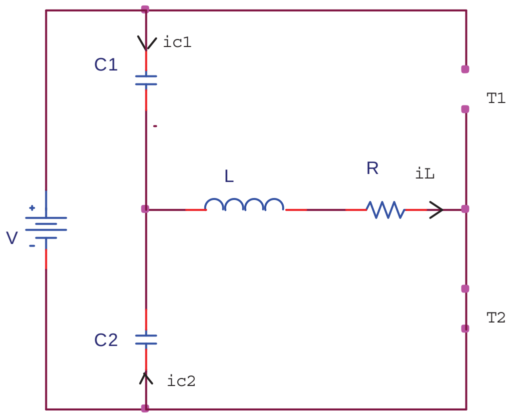


Fig. 5
In this mode only T_2 is turned-on

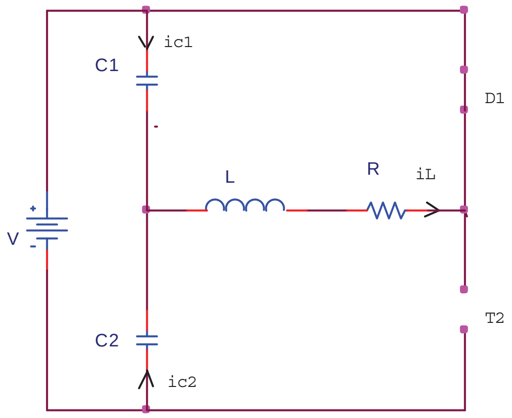
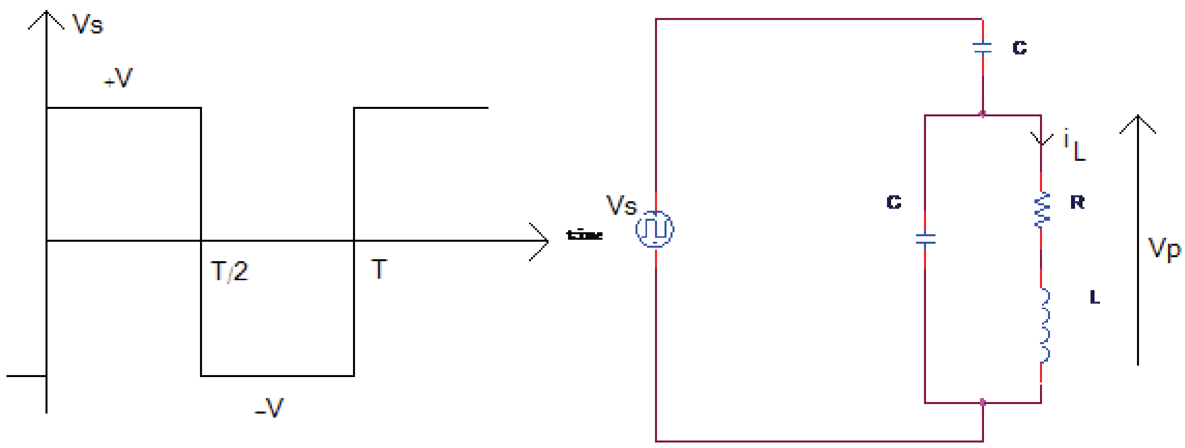


Fig. 6
(In this mode only D_1 is turned-on)



(a) **(b)**

Fig. 7
(a) Equivalent source voltage, (b) Complete equivalent circuit.

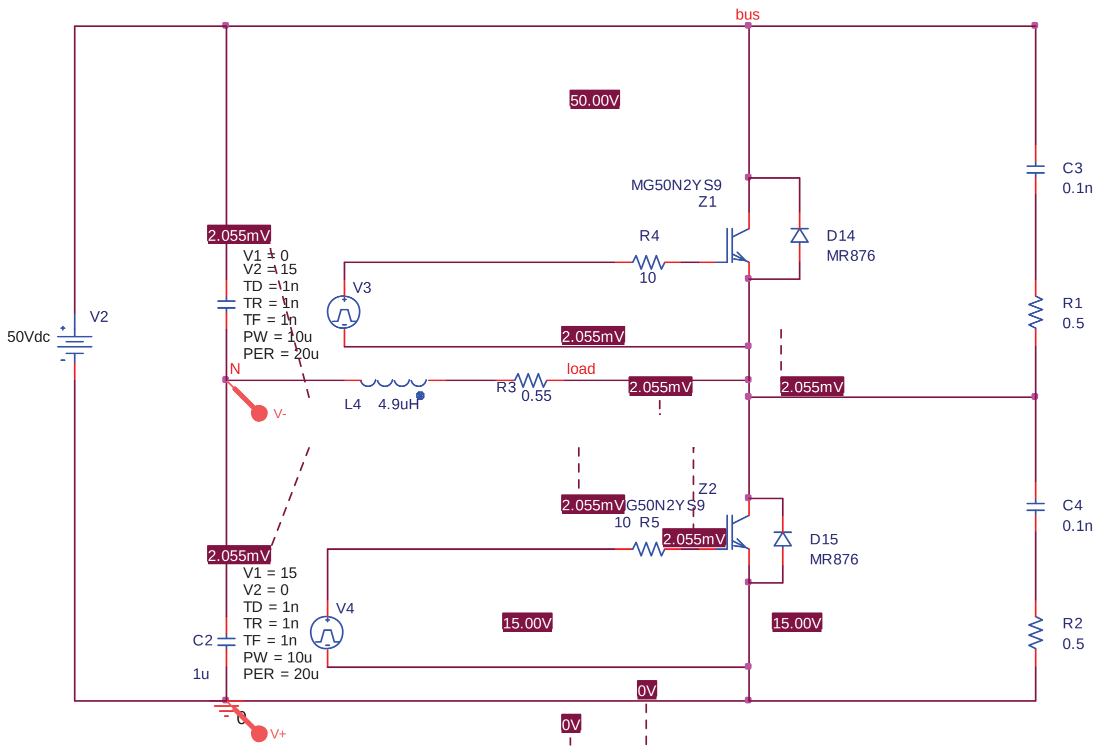


Fig. 8
The circuit used in the simulation

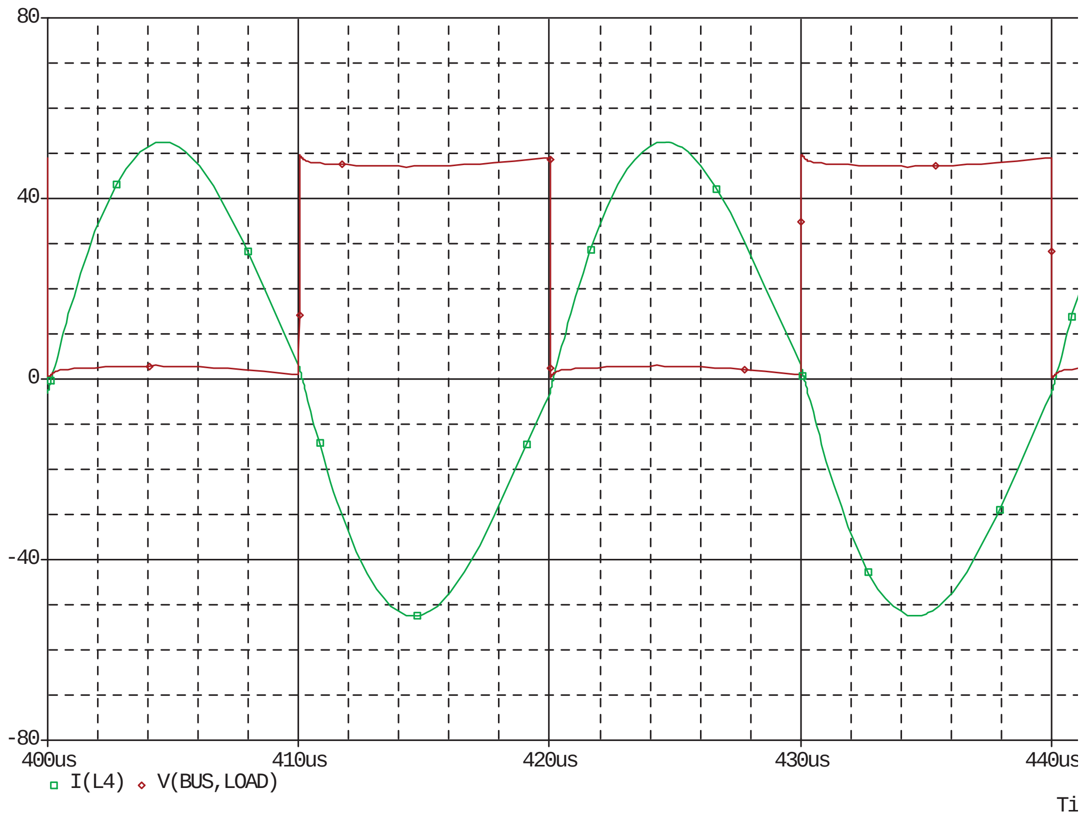


Fig. 9
The load current (I_L) and collector-emitter (V_{CE}) versus time

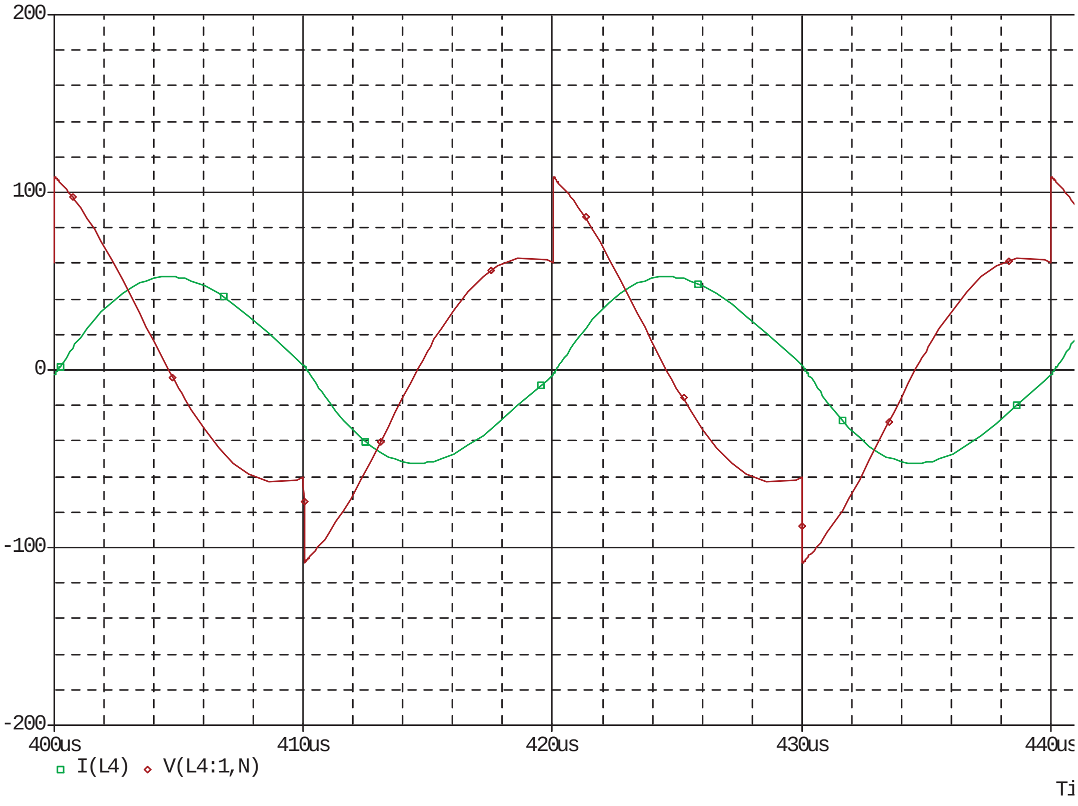


Fig.10
Load current (I_L) and load voltage (V_L) versus time

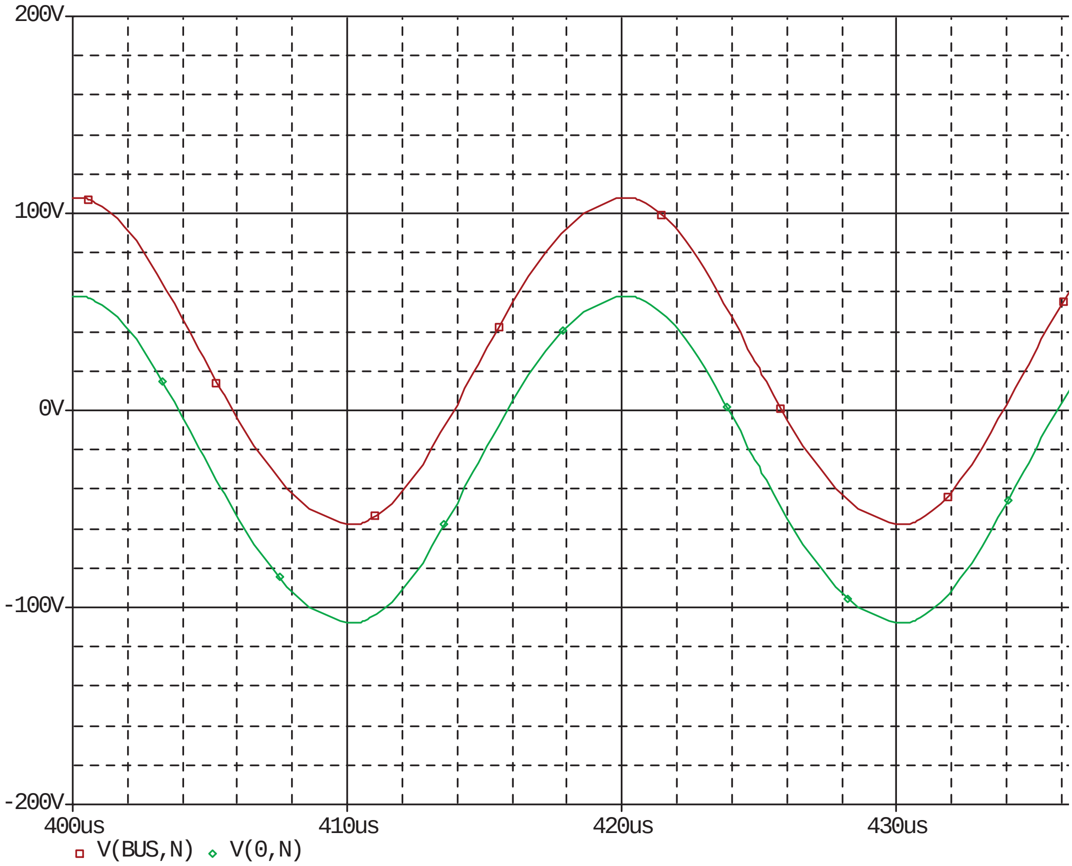


Fig. 11
The capacitor voltages V_{C1} (upper waveform) and V_{C2} (lower waveform) versus time.

Fig. 12
The gating signals

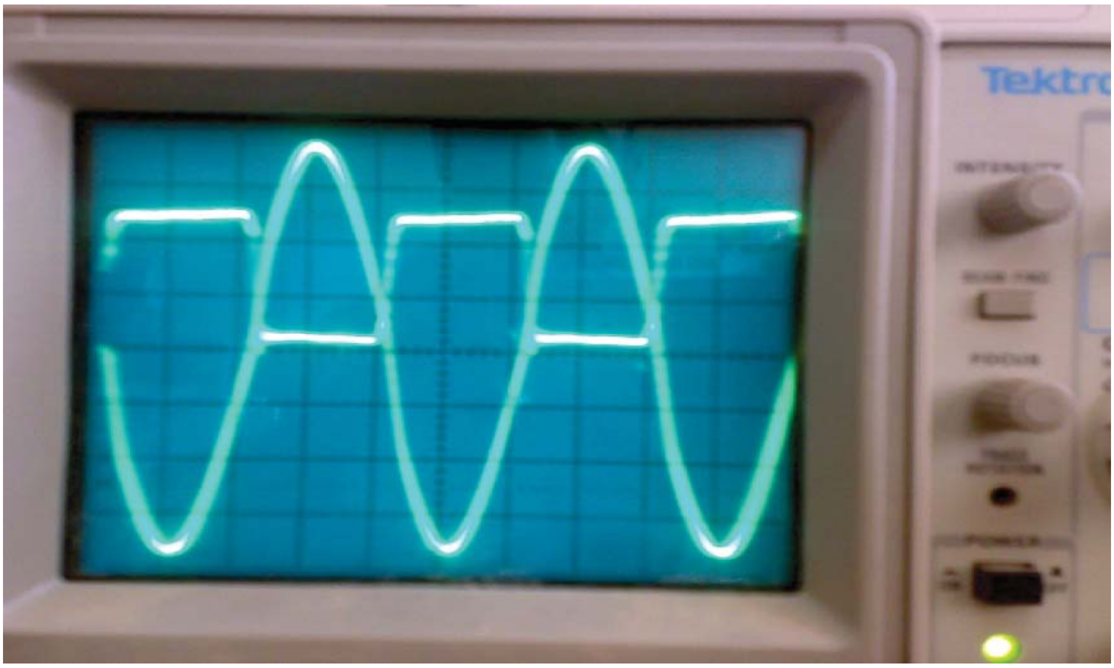


Fig. 13
The load current (I_L) and collector-emitter (V_{CE}) versus time

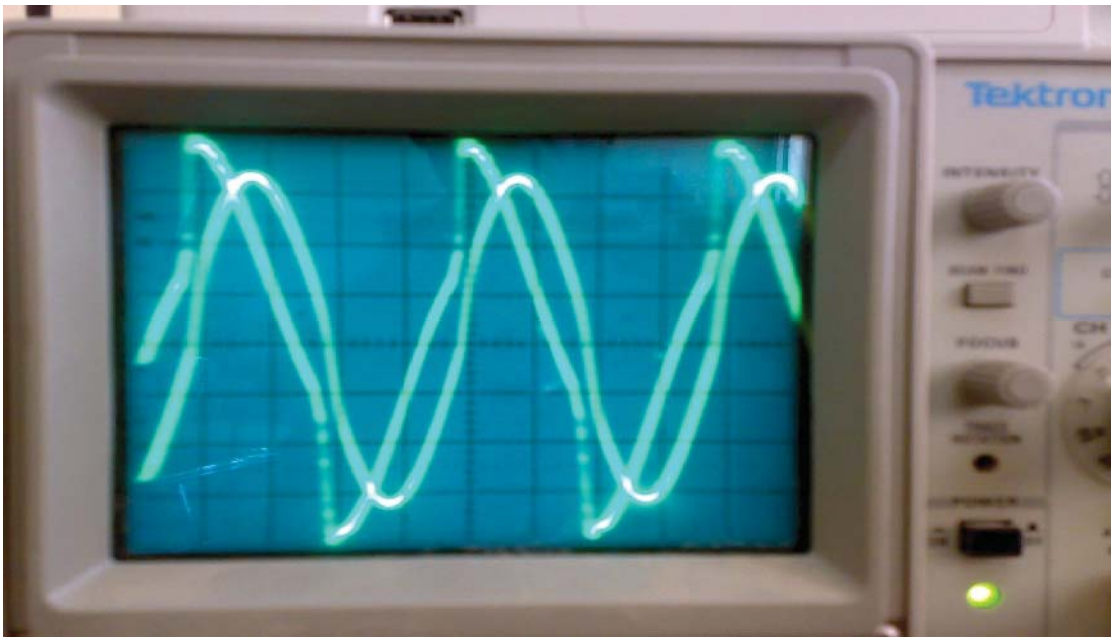


Fig.14
Load current (I_L) and load voltage (V_L) versus time.

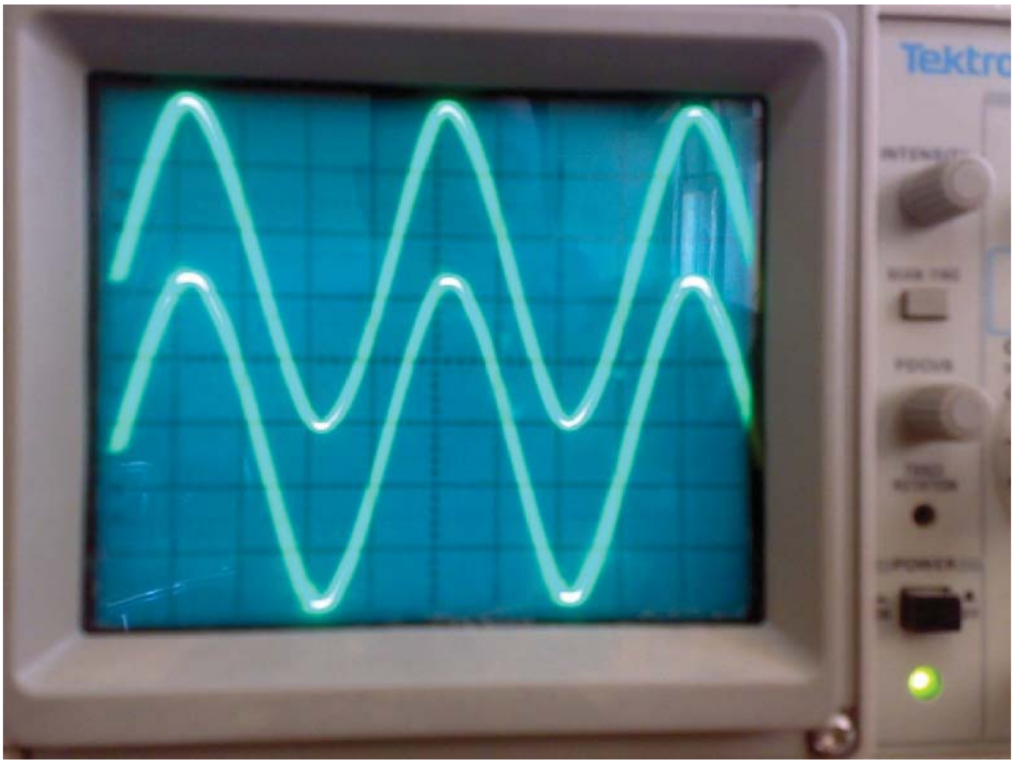


Fig. 15
The capacitor voltages V_{C1} and V_{C2} versus time.

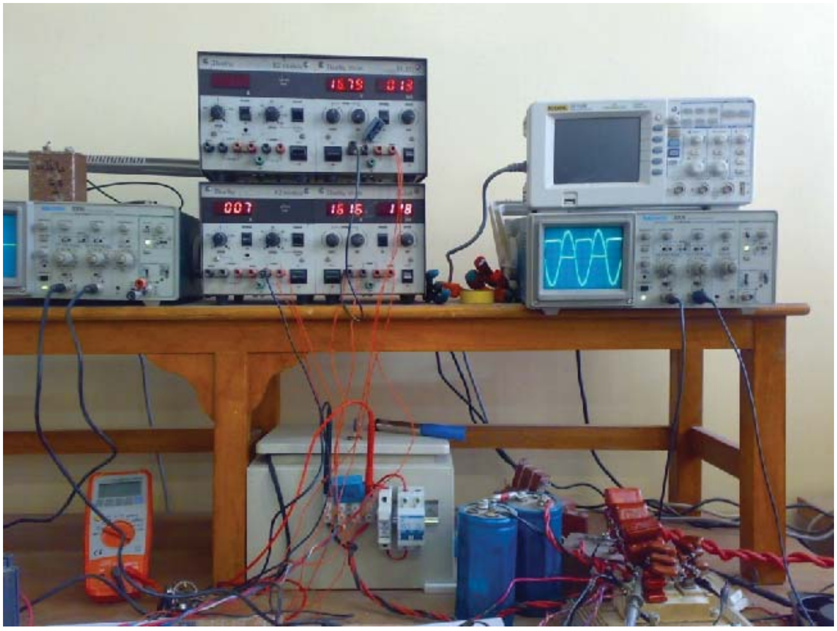


Fig. 16
A picture to part of the project

Fig. 17
The element in the coil is heated and reached the red color.

Fig. 18
The element in the coil is completely heated and brighten at a temperature of 700 C°.