Ultra-Wideband and Low Noise Transimpedance Amplifier

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Abstract— We present a new transimpedance amplifier (TIA) design possessing an improved bandwidth. This TIA employs a parallel combination of two series resonate circuits with different resonate frequencies on the conventional regulated common gate (RGC) architecture. In the proposed TIA, we employ the capacitance degeneration and series inductive peaking for pole-zero elimination. We implemented the layout of proposed TIA in a 0.18-µm CMOS process, where a 100-fF photodiode is considered. Our post-simulation test results show that the TIA provides 53-dBΩ transimpedance gain and 24-pA/$\sqrt{\mathbf{Hz}}$ input referred noise. The designed TIA consumes 11 mW from a 1.8-V supply, and its group-delay variation is 5-ps over 13-GHz 3-dB bandwidth.

Index Terms—Bandwidth, capacitance degeneration network, input-referred noise, photodiode-detecor (PD), regulated common gate (RCG) and transimpedance amplifier (TIA).

I. INTRODUCTION

Continuous growth in the wireless telecommunication has derived to high level of chip integration and focused research studies towards the field of high frequency applications [1]. The accelerated CMOS technology is the only candidate that can satisfy the demands for low-cost and high integration with reasonable speed for analog applications in the Giga-Hertz range [2].

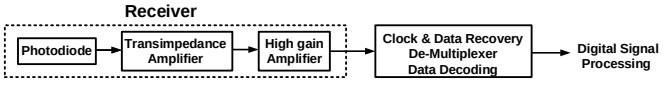

Fig. 1. Block diagram of an optical reciever.

The transimpedance amplifier (TIA) is the critical block in the optical communication system that converts the induced photodiode current into an amplified voltage signal to be used in the digital processing unit (Fig. 1). The bandwidth is considered as the highest priority in TIA design. The challenge in TIA design lies in the large photodiode parasitic capacitance Cpd, the input node that degrades the performances of the TIA. Therefore, it is required to decrease the input parasitic effects and prior to focusing on the compromise between the bandwidth and the noise [3, 4].

There have been two commonly used topologies in designing wideband CMOS TIAs: the common gate (CG) amplifier and the shunt feedback amplifier [5]. Several bandwidth enhancement efforts have been reported in published literature which were based on isolation of the input capacitance of the photodiode to minimize its effect on the bandwidth calculation. Inductive peaking is one of the commonly used techniques to improve the bandwidth and decrease parasitic capacitance effects [6]. Placing an inductor in a strategic location of the amplifier circuit provides a resonance with parasitic capacitances, which expands the bandwidth of the TIA [7-9]. Capacitive peaking has been used for bandwidth extension by using a capacitor to control the pole locations of a feedback amplifier [10, 11]. Multiple shunt parallel feedback is another approach for enhancing the bandwidth [12]. The effect of the photodiode capacitance can be more professionally reduced from the bandwidth limitation by using regulated cascode (RGC) [3].

In this work, we have proposed a new TIA design with improved bandwidth. The proposed TIA is based on modification of the input part of the conventional RGC TIA architecture by using parallel arrangement of two series resonate circuits with different resonate frequencies. Capacitance degeneration and series inductive peaking networks are used for pole-zero elimination to improve the bandwidth.

The paper is organized as follows: in Section II we present an overview of the traditional RCG input stag. The concept of modified RCG input stage and the analysis of the architecture of parallel arrangement of two series resonate circuits with different resonate frequencies are introduced. We present the capacitance degeneration architecture and proposed TIA design in Section III and Section IV, respectively. Finally, we present the noise analysis in Section V, demonstrative simulation results in Section VI, and the conclusions in Section VII.

II. REGULATED COMMON GATE (RCG) INPUT STAGE

A. *Conventional RCG Input Stage*

Among all the building blocks in an optical communication system, the TIA is the one of the most critical blocks in receiver design. It is a well-known fact that RGC input configuration can attain better isolation within the large photodiode capacitance C_{pd} by local feedback topology. Fig.2 shows the schematic diagram of the conventional RGC with a PD, which converts the incoming optical signal to a small signal rent I_{pd}. The common-source (CS) amplifier consists of M_1

and R_D operates as a local feedback technique and regulates the CG.

As a result of the small-signal analysis, the input resistance of the RGC circuit is given by [13] and [14].

$$Z_{i,RCG} = \frac{1}{g_{m2}(1+g_{m1}R_D)}, \quad (1)$$

where g_{m1} and g_{m2} are the transconducatnce of M_1 and M_2 respectively. It is clearly seen that the input resistance decreased because the transconductance G_m is $(1+g_{m1}R_D)$ times larger than that of CG amplifier input stage, where $1+g_{m1}R_D$ is the DC gain of the local feedback. Therefore, RGC stage acts as a buffer between the PD and the TIA stage and decreases the effect of the photodiode capacitance C_{pd} [14].

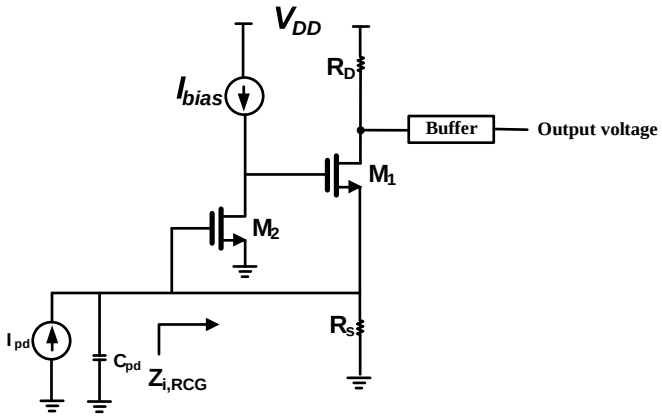

Fig. 2. Regulated common gate (RCG) TIA.

B. *Modified RCG Input Stage*

In the design of ultra-wideband TIAs, the wideband input stage plays very critical role. The design methodology of the narrow-band TIA is our first focus followed by demonstration of how to extend its input bandwidth.

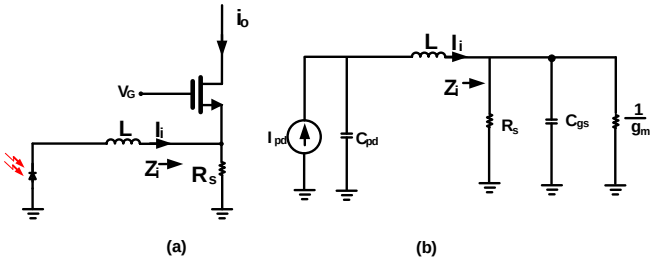

Fig. 3. The input part of a narrowband RCG TIA.

Fig. 3 shows the input part of a typical narrowband TIA topology. The RGC TIA topology improves the bandwidth limitation due to the input pole that consists of the gate-source capacitance (C_{gs}) and the input resistance (Z_i). Nevertheless, the large parasitic capacitance of photodiode C_{pd} still reduces both the bandwidth and the noise performance of the TIA.

The series inductive peaking technique is used to overcome this problem. The inductor L is placed between C_{gs} and of C_{pd}, which creates an inductive π network [14]. The expression used to analyze the performance of the current transfer function is derived from the small-signal mode circuit shown in Fig.3. (b).

$$\frac{I_i}{I_{pd}} = \frac{1}{s^3RC_{pd}C_{gs} + s^2LC_{gs} + sR(C_{pd}+C_{gs})+1} = \frac{1}{\left(\frac{s}{\omega_0}\right)^3\frac{k}{m}(1-k)+\left(\frac{s}{\omega_0}\right)^2\frac{1-k}{m}+\frac{s}{\omega_0}+1} \quad (2)$$

where $R = (1/g_m)//R_S$, $k = \frac{C_{gs}}{C_{pd}+C_{gs}}$, $m = \frac{R^2(C_{pd}+C_{gs})}{L}$ and the cutoff frequency $\omega_0 = \frac{1}{(C_{pd}+C_{gs})R}$. Inductive-peaking technique provides significant bandwidth extension ratio (BWER) by selecting different values for variables k and m [15].

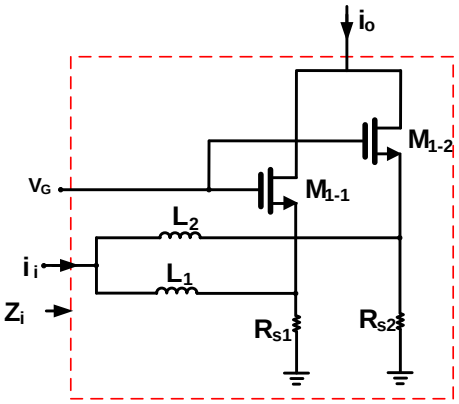

Fig. 4. The input part of RCG TIA with two input branches.

To improve the input-bandwidth, we use a parallel combination of two series resonate circuits with different resonate frequencies, as shown in Fig. 4. The input impedance is given by

$$Z_i = Z_1 // Z_2 \quad (3)$$

where

$$Z_j = \frac{R_j}{1+\omega_j^2 C_{gsj}^2 R_j^2} + j\frac{\omega_j^3 L_j C_{gs_j}^2 R_i^2 - \omega_j L_j C_{gs_j} R_j^2 + \omega_j L_j}{1+\omega_j^2 C_{gsj}^2 R_j^2}. \quad (4)$$

C_{gsj}, L_j and R_j are the gate –source capacitance , serial inductor and equivalent input resistance of transistor M_j , respectively $(j = 1, 2)$.

In (4), one should note that, if the reactive elements are accurately selected, then the input impedance become purely resistive. Moreover when the gate of M_{1-1} and M_{1-2} have the same bias voltages, M_{1-1} and M_{1-2} have identical cutoff frequency ω_0. As a result, the circuit can realize a wide bandwidth.

III. The Capacitance Degeneration

Modification of RGC input stage can be augmented through the possibility of achieving a broadband frequency response through the increment of the effective transconductance $G_m$of the circuit at high frequencies [5],[16]. To emphasize more on the above stated point, we can compensate the dominant pole of the overall circuit with a zero, which can be reached through capacitive degeneration configuration [14].

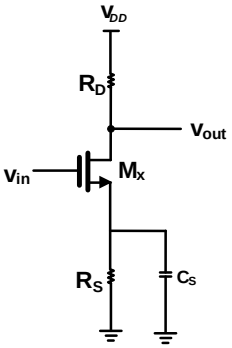

Fig.5. Configuration of capacitive degeneration.

For the capacitive degenenation toplogy shown in Fig.5, the transconductance equivalency is calculated as [17].

$$G_m = \frac{g_m}{1+g_m R_s}\,\frac{1+sR_sC_s}{1+s\dfrac{R_sC_s}{1+g_m R_s}} \qquad (5)$$

which introduces a zero (z_1) at $(R_sC_s)^{-1}$and a pole at $(1+g_mR_s)/R_sC_s$. The dominant pole can be compensated by the zero. As a result, the bandwidth is limited by the second lowest pole of the circuit.

The propsed capacitive degenartion toplogy shown in Fig.6 is employed to provide capacitive and resisitive degeneration. Therefore, extra gain and bandwidth enhancement can be achived at the same time.

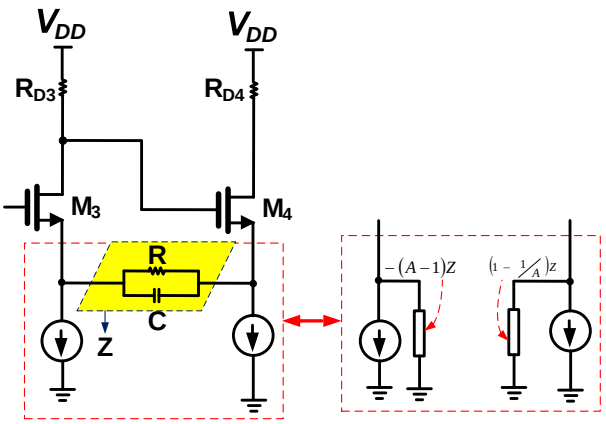

Fig.6. The proposed configuration of capacitive degeneration.

The transconductance equivalency of half of the circuit in Fig.5 is expressed as

$$G_m = \frac{g_m(1+sRC)}{1+g_m R/2 + sR_sC_s} \qquad (6)$$

Note that in (6), the transconductance introduces a zero (z_1) at $(R_sC_s)^{-1}$and brings an additional pole p_2 at $(1+g_m R/2)/R_sC_s$. The dominant pole $p_1 = \frac{1}{R_DC_L}$ appears at the drain node. If $R_sC_s = R_DC_L$, then the zero z_1 cancels the pole p_1, therefore the bandwidth is extended to the second pole of the circuit $p_2 = (1+g_m R/2)/R_sC_s$.

In pole-zero elimination technique, if the zero is moved to a lower frequency (C large), the frequency response displays a source peaking so that the capacitor should be small to avoid the gain peaking.

This is an important advantage of the intended circuit stems from the variation of the amplifier's input impendance and thus the proceeding stage load is seen.

IV. The Proposed TIA

We present the proposed wideband TIA based on RCG in Fig. 7. The modification of the input network of RCG TIA provides better enhancement of bandwidth and decreases the input-referred noise current. A 100-fF photodiode capacitor is

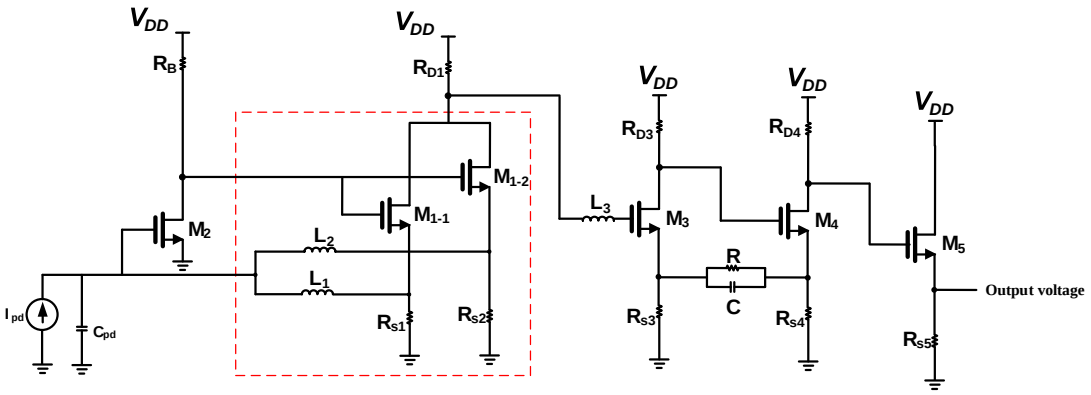

Fig.7. Schematic of proposed RCG TIA.

used at the input of the TIA. The gain stage is composed of two common source amplifiers with capacitance degeneration technique.

Referreing to Miller theorem [18], the shunt impedance $Z = (R//(1/sC))$ connected between the drain nodes of M_3 and M_4 can be separated into a couple of grounded impedances. If A is the voltage gain between the two terminals of Z in Fig.5, then the equivalent split impedances are $-(A-1)Z$ and $\left[\left(1-{}^{1}/_{A}\right)Z\right]$. These impedances produce zeros with R_{s3} and R_{s4} to make perfect cancellation of the poles at the drain of M_3 and M_4. Therefore, the bandwidth is further improved [14].

The source follower consisting of M_5 and R_{s5} as a buffer is used to evade affecting the frequency response of the TIA due to input parasitic capacitances of the succeeding stage in the receiver system namely, the Limiting Amplifier (LA).

V. NOISE ANALYSIS

In the proposed TIA of Fig. 6, we consider the thermal noise generated by the active devices (M_{1-1}, M_{1-2} and M_2) and thermal noises of resistors (R_B,R_{s1}, R_{s2} and R_D). The flicker noise $\left({}^{1}/_{f}\right)$ is ignored because it is not dominant in MOS transistor. The noise contribution of R_D is neglected due to the parasitic capacitance in parallel with R_D which makes its noise impact non dominant. The noise analysis is performed based on the noise model shown in Fig.7.

The thermal noise in MOS transistor is modeled by a noise current source between the drain and source terminals with spectral noise of [19]

$$\overline{i_{n,d}^2} = 4k_B T\gamma g_m, \tag{7}$$

where k_B is the Boltzmann's constant (J/°K), T is the absolute temperature (°K) and γ is the complex function of transistor parameters and bias conduction. The equivalent input noise current spectral density can be given as

$$\overline{i_{n,in}^2} \approx \overline{i_{n,R}^2}\cdot x^2\left[\left(1-\omega^2 L_1 C_{pd}\right)^2+\left(1-\omega^2 L_2 C_{pd}\right)^2\right] + \omega^2 C_{pd}^2\left(\overline{i_{n,M1-1}^2}+\overline{i_{n,M1-2}^2}+\overline{i_{n,M2}^2}\right), \tag{8}$$

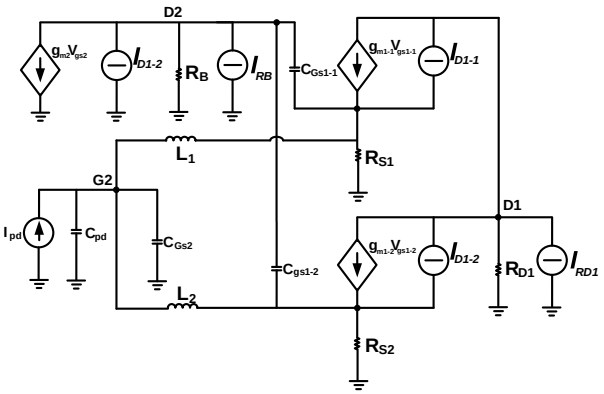

Fig.8. Modified RCG TIA with noise sources.

where $\overline{i_{n,R}^2}$ is the thermal noise of the resistors given by

$$\overline{i_{n,R}^2} \approx 4kT\left\{\left(\frac{1}{R_{S1}}+\frac{1}{R_{S2}}+\frac{\left(\gamma g_{m2}+{}^{1}/_{R_B}\right)}{\left(g_{m2}+{}^{1}/_{R_B}\right)^2}\times\left(\frac{1}{R_{S1}^{\,2}}+\frac{1}{R_{S2}^{\,2}}\right)\right)\right\} \tag{9}$$

and

$$x = 1-\omega^2\frac{L_1+L_2}{1+g_{m2}R_B}\left(C_{gd2}+\frac{Cgs_2}{1+g_{m2}R_B}\right) \tag{10}$$

$$\overline{i_{n,M1-j}^2} = \frac{4kT\left(\gamma g_{m1-j}+{}^{1}/_{R_D}\right)}{g_{m1-i}^2}, \quad (j=1,2)$$

$$\overline{i_{n,M2}^2} = \frac{4kT\left(\gamma g_{m2}+{}^{1}/_{R_B}\right)}{\left(g_{m2}+{}^{1}/_{R_B}\right)^2}. \tag{11}$$

For half circuit of the capacitive degeneration stage, the input noise current spectral density $\left(\overline{i_{n,HCDEG}^2}\right)$ is given by

$$\overline{i_{n,HCDEG}^2} = \frac{4kT\omega^2 C_{Dj,eq}{}^2}{1+\omega^2 R_{sj,eq}^2 C_{sj,eq}^2}\left[\left(\gamma g_{d0,j} + 1/R_{Dj}\right)\left(\frac{1+g_{mj}+R_{sj,eq}}{g_{mi}}\right)+R_{sj,eq}^2\right],\ j=3,4 \quad (12)$$

where $C_{Dj,eq}$ and $C_{Dj,eq}$ are the equivalent parasitic capacitance at drain and source nodes respectively, $R_{sj,eq}$ is the equivalent resistance at source node and $g_{do,j}$ is the zero-bias drain conductance. Because the main deliberation is given to the modified RCG input stage and the capacitive degeneration stage, the contribution noise of the buffer is ignored, As shown in (7), the resistors noise is the main noise at low frequencies and the impact noise of $M_1$and M_2 becomes dominant at high frequencies. Note that the input noise current reduces appreciably at high frequencies using L_1 and L_2 at the input of the TIA. Furthermore the minimum noise can be realized by boosting the transconductance g_{m2}.

VI. Simulation Results

We performed simulation analysis of the proposed TIA circuit using Cadence tools. Simulations are done by utilizing RF transistor model based on 0.18µm HV CMOS technology with a 1.8-V single supply and a 100-fF photodiode capacitance. Fig.9 shows the layout of the proposed TIA with 147µm × 230µm of area cost. The frequency responses of the conventional RCG and the proposed TIAs are presented in Fig.10. The RCG TIA provides a bandwidth of 3.5 GHz, whereas the bandwidth of proposed TIA extends up to 13 GHz. Transimpedance gains of the conventional RCG and proposed TIAs are 47.7 dBΩ and 53.2 dBΩ, respectively. While the total power consumption of the conventional RCG TIA is 5 mW, the proposed TIA consumes only 11 mW.

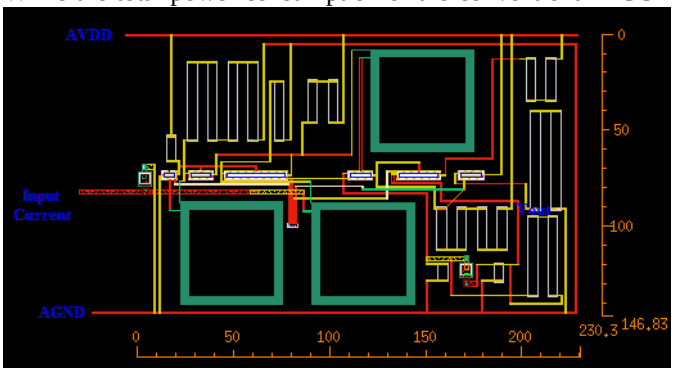

Fig.9. The layout of the proposed TIA

Fig.11 shows the simulation results of input noise current spectral densities of the RCG and the proposed TIA. As shown, the proposed TIA has less input referred noise current than the RGC configuration. It shows an average input noise current spectral density below $24\text{pA}/\sqrt{\text{Hz}}$ within the bandwidth.

Fig. 12 shows the group-delay variation with frequency. As shown, the proposed TIA provides smaller group-delay variation than the RGC configuration.

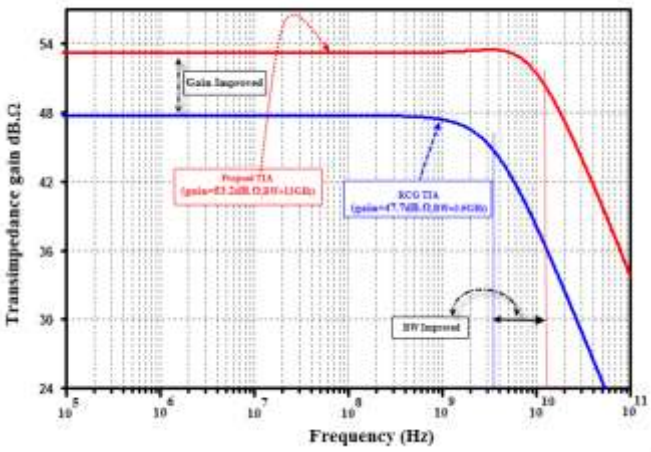

Fig. 10. Frequency response results of the TIA

The TIA has a minimum group delay of 4 ps, increases to 14 ps within the bandwidth of 13 GHz. This small variation means that output signal will not suffer from distortion as RGC TIA.

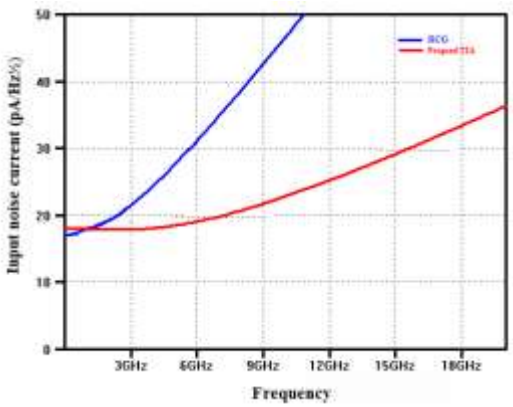

Fig.11. Spectral density of the input noise curren

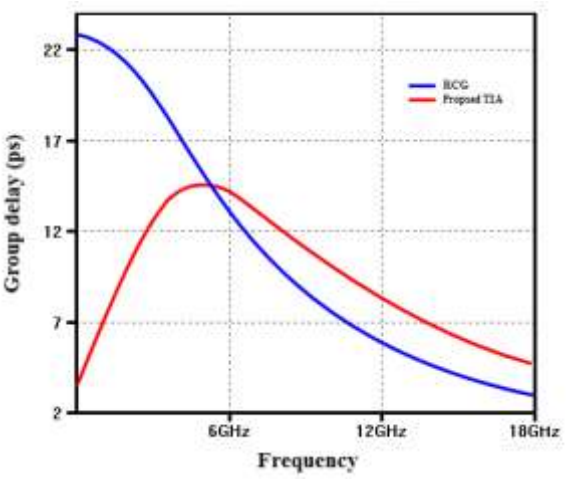

Fig.12. The group delay variation of TIA.

The transient response of the TIA is shown in Fig.13 at different process corners. The width of the input current pulse is 10 ps with a rise/fall time of 1 ps and the peak-to-peak current is 50 µA. The simulation result shows that, at different process

corners, the output swing variations is very small. This depicts that the transient response of the TIA is fast enough even for small inpt current.

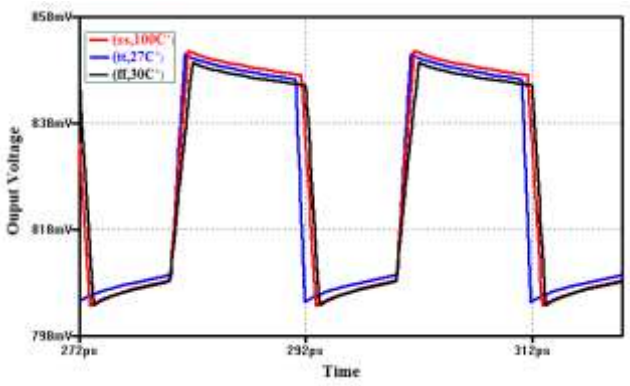

Fig.13. Transient response of the TIA at different process corners.

Table 1. Performance summery and comparison with the other works using (180nm CMOS) technology

Parameter	[20]	[16]	[21]	[22]	[23]	This Work
Gain (dB)	59	53	54	62.3	51	53.2
BW (GHz)	8.6	8	7	9	30.5	13
C_{PD} (fF)	150	250	300	150	50	100
Power (mW)	18	13.5	18.6	108	60.1	11
Noise $pA/\sqrt{Hz}$	25	18	18	-	55.7	24

Table 1 shows a comparison of the proposed TIA performance with other works. It can be seen that the noise of the proposed TIA is smaller than the other TIA configurations, where the active inductors have been used. In addition, the power consumption is comparatively smaller than the other TIA circuits.

VII. Conclusion

The proposed TIA design improves the performance of the RGC TIA. Use of parallel combination of two series resonate circuits with different resonate frequencies improves the bandwidth and minimizes the equivalent input noise current density of RCG TIA. The capacitance degeneration and series inductive peaking networks are used for pole-zero elimination. The proposed design is implemented in a 0.18-µm CMOS process in the presence of a 100fF photodiode capacitance. It is observed that the TIA achieves a -3-dB bandwidth at 13GHz and transimpedance gain of 53.2 dBΩ. The input referred noise current spectral density is $24pA/\sqrt{Hz}$ and the average group-delay variation is 5 ps over the 3-dB bandwidth and the TIA consumes 11 mW from a 1.8 V supply. Simulation results show that the TIA displays a broadband flat response, provides an ultra-low noise performance, and hence it is proficient for applications in optical transceivers.

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