Digital Simulation of an Interline Dynamic Voltage Restorer for Voltage Compensation

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Abstract – The Dynamic Voltage Restorer (DVR) provides an advanced solution for voltage sag/swell problems. The voltage-restoration process involves real-power injection into the distribution system. The Interline DVR (IDVR) proposed in this paper provides a way to compensate the voltage sag/swell caused in a feeder. The IDVR consists of several DVRs connected to different distribution feeders in the power system sharing common energy storage, where one DVR in the IDVR system works in voltage-sag/swell compensation mode while the other DVR in the IDVR system operate in power-flow control mode. The modelling and simulation of single phase IDVR system using Sinusoidal Pulse Width Modulation (SPWM) technique for voltage sag and swell conditions and three phase IDVR using Space Vector Pulse width modulation (SVPWM) technique for voltage sag condition are presented. Closed loop control for voltage sag and swell for a simple IDVR systems are modeled and simulated using MATLAB software. The simulation results are presented to demonstrate the effectiveness of the proposed IDVR system.
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Index Terms— Interline Dynamic Voltage Restorer (IDVR), Interline Power Flow Controller (IPFC), Sinusoidal Pulse width modulation (SPWM), Space Vector Pulse width modulation (SVPWM), Total Harmonic Distortion (THD).

I INTRODUCTION

The need of the electrical power is increasing and simultaneously the problems while transmitting the power through the distribution system are also increasing. Voltage fluctuations are considered as one of the most severe power quality disturbances to be dealt with. Even a short-duration voltage fluctuation could cause a malfunction or a failure of a continuous process. There are several types of voltage fluctuation that can cause the systems to malfunction, including surges and spikes, sag, swell, harmonic distortions, and momentary disruptions. Among them, voltage sag and swell are the major power-quality problems. Voltage swell is the sudden increase of voltage to bout more than 110% amplitude of the supply voltage, whereas the voltage sag is the sudden decrease of voltage ton about 90% amplitude of supply voltage. This is caused due to the sudden reduction or addition of the load across that particular feeder. This change of voltage is compensated by injecting the voltage in series with the supply from another feeder at the time of disturbances using DVR. This IDVR system is presently one of the most cost-effective and a highly efficient method to mitigate voltage sag/swell.

The concept of Interline Dynamic Voltage Restorer (IDVR) where two or more voltage restorers are connected such that they share a common DC-link is similar to the Interline Power Flow Controller (IPFC) concept. In this paper, a two-line IDVR system is explained which employs two DVRs, connected to a common DC-link, is connected to two different feeders originating from two grid substations, and could be of the same or different voltage level. When one of the DVRs compensates for voltage swell/sag produced, the other DVR in IDVR system operates in power-flow control mode.

DVR principles and voltage restoration methods at the point of common coupling are presented. The problem of voltage sags and swells and its severe impact on sensitive loads are described [1]. Voltage swell and overvoltage compensation problems in a diode bridge rectifier supported transformer-less coupled DVR, are discussed. The simulation and experimental results for unbalanced voltage swell compensation are given [2]. The performance of a DVR in mitigating voltage sags/ swells is demonstrated with the help of MATLAB. The DVR handles both balanced and unbalanced situations [3].

The modeling and simulation of IDVR is presented in paper [4] and [6]. Paper [5] proposed a new topology based on the Z source inverter for the DVR, in order to enhance the voltage restoration property of the device. The modeling aspects of the DVR working against voltage sags by simulation in the PSCAD/EMTDC have been presented [7]. Modeling

and simulation of single phase IDVR using multiple PWM technique is presented [8] and [10].The modeling and simulation of single phase Z source impedance based DVR, IDVR using multiple PWM technique is presented [9] and [13]. In this paper, modeling and simulation of single phase IDVR with SPWM technique is used for voltage sag and swell compensation.

II. PRINCIPLE OF IDVR

The IDVR system consists of several DVRs in different feeders, sharing a common DC-link. A two-line IDVR system shown in Fig.1 employs two DVRs are connected to two different feeders where one of the DVRs compensates for voltage swell/sag produced, the other DVR in IDVR system operates in power-flow control mode. The common capacitor connected between the two feeders act as the common DC supply.

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Voltage swell/sag in a transmission system are likely to propagate to larger electrical distance than that in a distribution system. Due to these factors, the two feeders of the IDVR system in Fig.1 are considered to be connected to two different grid substations. It is assumed that the voltage distortion in Feeder$_1$ would have a lesser impact on Feeder$_2$.

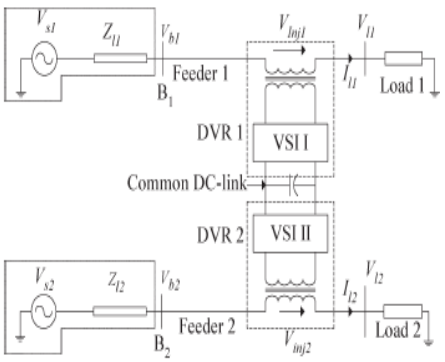

Fig.1 Schematic diagram of an IDVR

The upstream generation-transmission system is applied and the two feeders can be considered as two independent sources. These two voltage sources V_{s1} and V_{s2} are connected in series with the line impedances Z_{l1} and Z_{l2} which is in-turn connected to the buses B_1 and B_2 as in Fig. 1. The DVR is connected in series with the feeder and the DVRs across different feeders are connected by a common DC-link. The load across each feeder is connected in series to the DVR, where V_{l1} and V_{l2} are the voltages across the load.

The injection of an appropriate voltage needs a certain amount of real and reactive power which must be supplied by the DVR. Supply of real power is met by means of an energy storage facility connected in the DC-link. Large capacitors are used as a source of energy storage in most of the DVRs. Generally, capacitors are used to generate reactive power in an AC power system. However, in a DC system, capacitors can be used to store energy. When the energy is drawn from the energy storage capacitors, the capacitor terminal voltage decreases. Hence, large capacitors in the DC-link energy storage are needed to effectively mitigate voltage swell of large depths and long durations. The pulse can be generated using various modulation techniques. In this paper, the pulse for the switch is generated using SPWM.

III. MODEL OF IDVR USING SPWM TECHNIQUE

The simulink models of the closed loop controlled IDVR system with the H bridge inverter using SPWM technique for sag and swell conditions are developed and the simulation results are presented. The IDVR system with two back-to-back connected DVR stations was implemented with a closed loop control of inverter switches. Fig.2 shows the simulink model of the closed loop controlled IDVR. The rectifier-inverter system is shown as a subsystem.

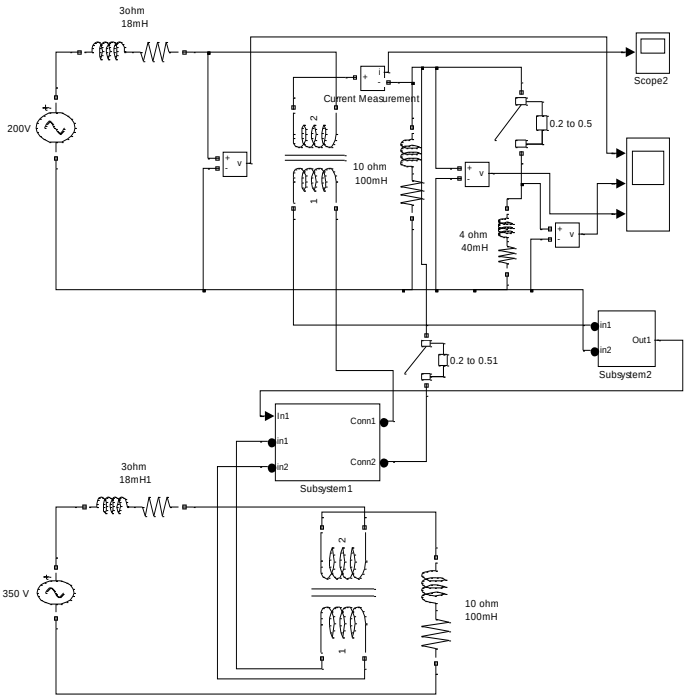

Fig.2 Simulation Circuit of IDVR

The subsystem 1 consists of a full bridge inverter with a filter. Subsystem 2, shows the rectifier output voltage The SPWM control technique is used to reduce the harmonic content in the output voltage. The driving sine pulses for the switches are shown in Fig.3.

Fig.4 (a) shows a 32.6 % voltage sag initiated at 300ms and it is kept until 600ms, with a total voltage sag duration of 300ms in low voltage feeder 1. Fig.3 (b) and (c) show the voltage injected by the DVR 2 and the compensated load voltage respectively. Due to the presence of the IDVR, the load voltage remains constant throughout the voltage sag period. Fig.5 shows the common DC link voltage waveform. Fig.6 shows the FFT analysis of the closed loop IDVR system for sag. The Total Harmonic Distortion (THD) value is 4.81%.

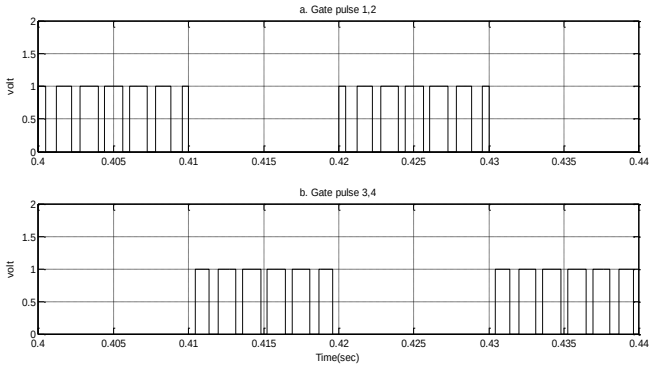

Fig.3 Driving pulses of inverter switches

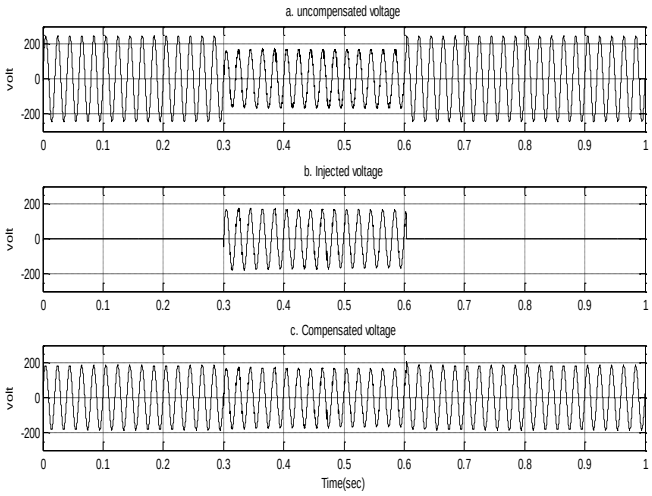

Fig.4 Response of IDVR to a voltage sag

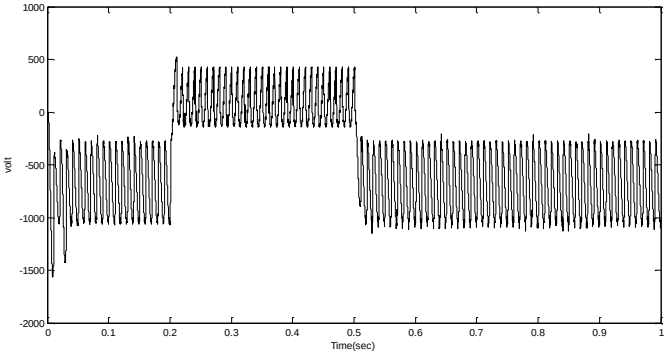

Fig.5 Common DC link voltage for sag

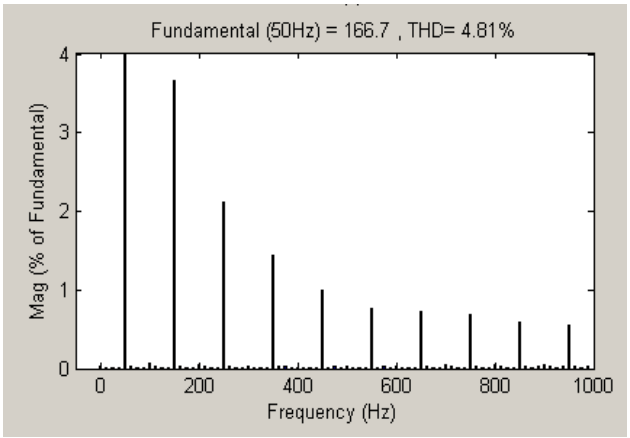

Fig.6 FFT analysis of IDVR for sag

Fig.7 (a) shows a 44.1 % voltage swell initiated at 300ms and it is kept until 600ms, with a total voltage swell duration of 300ms in low voltage feeder 1. Fig.7 (b) and (c) show the voltage injected by the DVR 2 and the compensated load voltage respectively. Due to the presence of the IDVR, the load voltage remains constant throughout the voltage swell period. Fig.8 shows the common DC link voltage waveform. Fig.9 shows the FFT analysis of the closed loop IDVR system for swell. The Total Harmonic Distortion (THD) value is 0.12%.

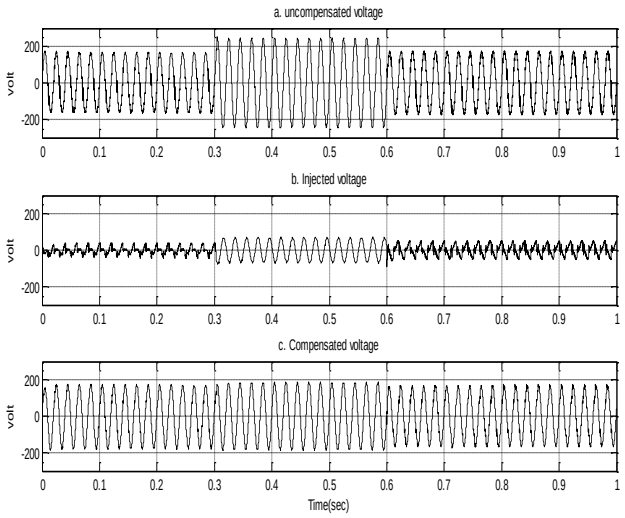

Fig.7 Response of IDVR to a voltage swell

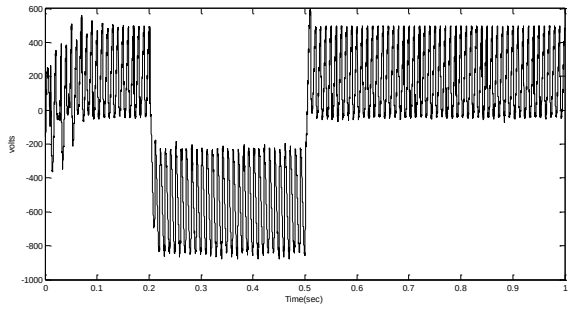

Fig.8 Common DC link voltage for swell

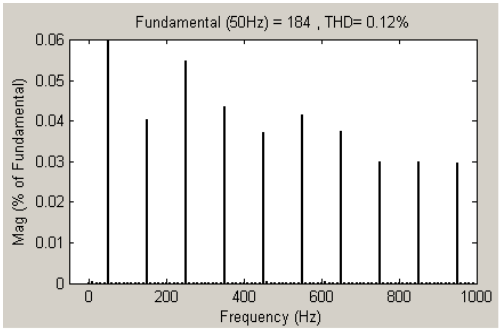

Fig.9 FFT analysis of IDVR for swell

IV. IDVR USING SVPWM TECHNIQUE

The proposed IDVR circuit with the Space Vector PWM is shown in Fig.10. Here, the error voltage in the dq-frame is used to calculate the resultant reference voltage and angle α of the space vector eight sector frame work. Table. 1 shows the parameters used for simulation studies.

The subsystem 1 consists of feeder 1 and DVR 1 as shown in Fig.12. The DVR 1 consists of an inverter, switching time calculator and switching pulse generator. The subsystem 2 consists of feeder 2 and DVR 2. The DVR 2 has an inverter, switching time calculator and switching pulse generator.

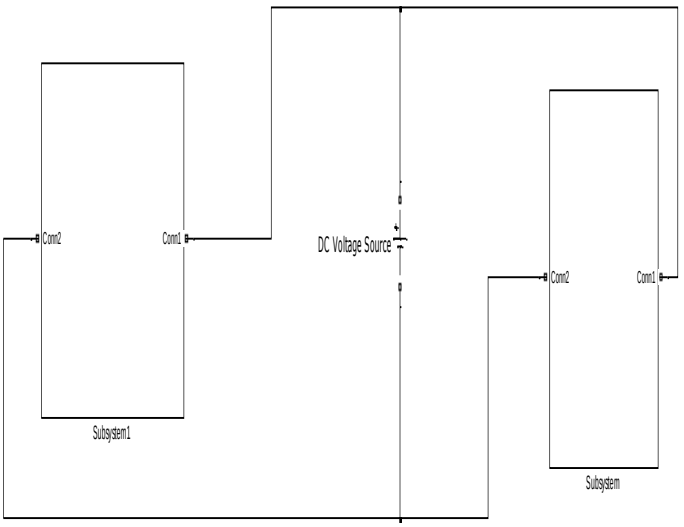

Fig. 10 Simulation circuit of three phase IDVR

Table. 1 Parameters of the two line IDVR

Supply voltage feeder 1	240V
Supply voltage feeder 2	707V
Source Impedance	(0.1+j3.142*e-4)Ω
Line impedance (for 100km)	(1.6+j0.34)Ω
Series transformer turns ratio	1:1
Injection transformer ratio	1:1
DC voltage	260V
Fixed Load resistance	40Ω
Fixed Load inductance	60mH
Filter inductance	10mH
Filter capacitance	0.0177μF
Line frequency	50Hz
Carrier frequency	12003Hz

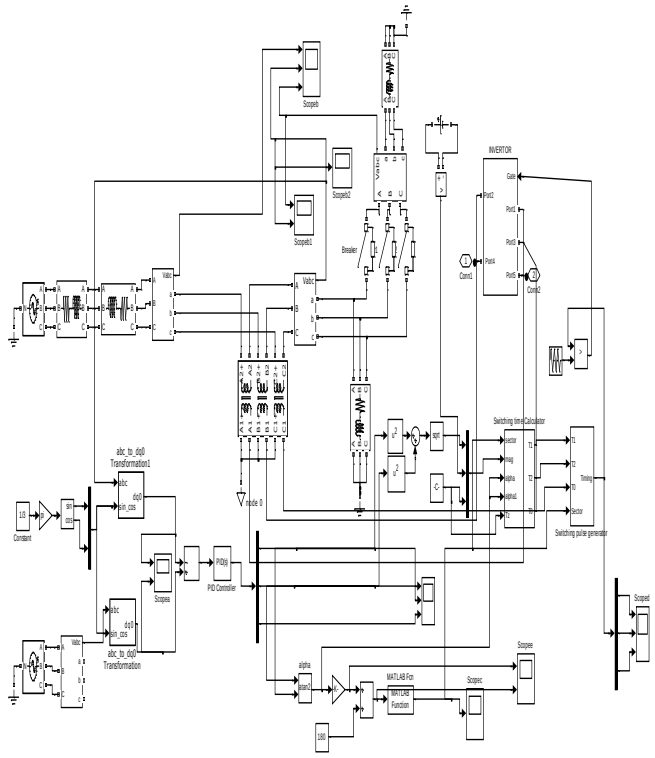

Fig.12 Subsystem 1 of three phase IDVR

Fig.13 indicates that 27.42% voltage sag is initiated at 300ms and it is kept until 800ms, with a total voltage sag duration of 500ms in the low voltage feeder 1. Fig.14 (a) and (b) show the voltage injected by the DVR2 and the compensated load voltage respectively. Due to the presence of the IDVR, the load voltage remains constant throughout the voltage sag period. Fig.15 shows the FFT analysis of the three phase IDVR with the SVPWM model. The THD of the SVPWM system is found to be 0.08 %.

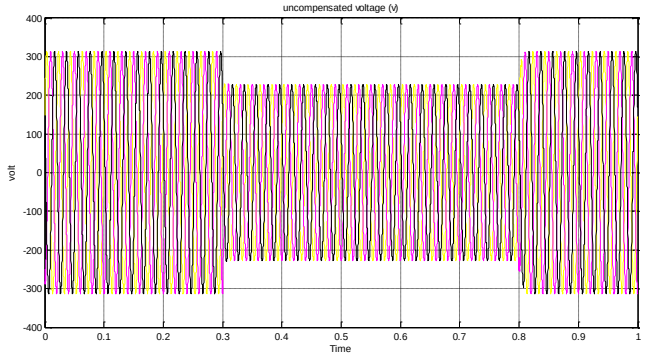

Fig.13 Voltage sag of three phase IDVR

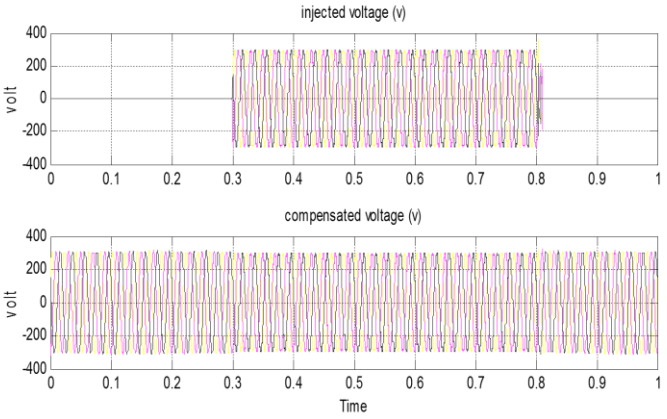

Fig.14 Response of three phase IDVR to a voltage sag

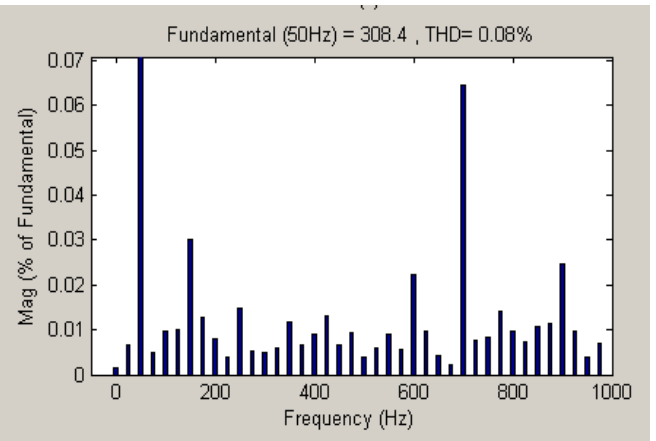

Fig.15 FFT analysis of the three phase IDVR

V. CONCLUSION

The modelling and simulation of single phase IDVR system using SPWM technique for sag and swell conditions are presented. The modelling and simulation results of three phase IDVR using space vector PWM technique are also presented. The model of single phase IDVR for 44.1% of the voltage swell and 32.6% of the voltage sag is compensated using closed loop control. The model of three phase IDVR for 27.42% of the voltage sag is compensated using closed loop control. The simulation results indicate that the implemented control strategy compensates voltage sags with high accuracy. The results show that the control technique is an improved method for voltage sag and swell compensation.

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