Analysis of Device Mismatches Effect on the Performance of UWB Receiver Front-End in Wireless Body Area Network Sensor Nodes

Thaar A.Kareem[1,2(✉)], Saif Benali[1], Hatem Trabelsi[1]
[1] Electrical Engineering Department, University of Sfax, Sfax, Tunisia
[2] University of Misan, Misan, Iraq
`thaar_kareem@uomisan.edu.iq`

Abstract—Today it is important to manufacture high quality integrated circuits which are insensitive to device mismatches. This paper presents an analysis of MOSFET transistors mismatches effect on the performance of UWB receiver front-end which constitute the most important part of Wireless Body Area Network sensor node. The receiver is based on Balun LNA with 25% fully differential double-balanced passive mixer. A PMOS and NMOS transistors mismatch models were proposed to determine LNA output offset voltage and mixer offset current respectively. The analysis result suggests that, to minimize NMOS current mismatch, and thus reducing second-order inter modulation distortion, the overdrive voltage $V_{GS} - V_{th}$ must be maximized. A Monte Carlo and harmonic balance simulations were performed using $0.18\mu m$ CMOS process to evaluate the impact of $W/_L$ mismatch as well as V_{th} mismatch on the receiver gain and IIP2. Simulation results show that IIP2 of the receiver is less sensitive to mixer NMOS mismatch but receiver gain is more sensitive. The receiver IIP2 confidence interval in case of NMOS $W/_L$ mismatch is [24.674, 24.77]dBm and in case of NMOS V_{th} mismatch is [24.659, 24.857]dBm. This show the robustness of the proposed UWB receiver front end. Therefore, the proposed circuit meets the requirement of UWB system perfectly which make it suitable for WBAN applications.

Keywords—WBAN UWB receiver, LNA, passive mixer, transistor mismatch, Monte Carlo

1 Introduction

For the purpose of monitoring physiological signal, the Ultra-Wide Band-Wireless Body Area Network (UWB-WBAN) is acknowledged to provide efficient, low power, and optimized wireless communication between sensor nodes implanted in or worn on the human body [1]. The Federal Communications Committee (FCC) mask limits UWB emission power in this application to less than -41.3 dBm/MHz in the 3.1-10.6 GHz band to avoid potential interference with already-existing applications [2].

Thus, it is necessary to design integrated circuits with high immunity to process, voltage, and temperature (PVT) variations in order to guarantee stable operation over these variations [3].

The Receiver Front-End (LNA+ Mixer) is one of the key elements of the UWB sensor nodes.

When studying differential LNA and Mixer circuits, we make the assumption that the bias currents and characteristics of identical transistors are the same. In practice, MOS devices have a mismatched threshold voltage (Vth) since Vth is dependent on the surface charge density, oxide thickness, gate material, and substrate doping. Dopants are incorporated into the channel and gate areas of the transistor during manufacturing to modify Vth. The doping levels differ erratically from transistor to transistor [4].

Additionally, random variation affects two identical MOS transistors, leading to mismatches in the W/L ratio. Mismatched Vth and W/L ratios cause DC to offset at the circuit nodes. This might cause the circuit's stages to operate nonlinearly or get saturated [5][6].

Time-independent random differences in physical quantities of similarly designed devices are caused by processing-induced device mismatch. As device dimensions shrink and the available signal swing shrinks, the impact of MOS transistor mismatch becomes increasingly significant. For precise analog circuit design, the mismatch is a critical design parameter [7].

The mismatch of two CMOS identical transistors is characterized by the random variation of the difference in their threshold voltage Vth , their body factor, and their current factor.

The second order intercept point (IIP2) of a direct conversion receiver system is a critical performance parameter. It is a measure of second order non-linearity and helps quantify the receiver's susceptibility to single and 2-tone interfering signals. At high frequencies, due to the presence of parasitic capacitance, the linearity (IIP2) drops[8].

In this paper, we will present an analysis of how device mismatches affect the performance of the UWB receiver front-end.

This paper is organized as follows: The receiver architecture front-end is presented in Section 2. The mismatch in PMOS transistors and its effect on LNA performances is analyzed in Section 3. Mismatch analysis in the receiver front-end and Monte Carlo simulation results with random variation in size and voltage threshold of mixer NMOS switches are detailed in Section 4. Section 5 concludes this paper.

2 Receiver architecture

The transceiver architecture is shown in Figure 1. Hardware minimization can be achieved by using a direct conversion architecture that eliminates the image-reject filter and other IF components, enabling a monolithic transceiver [9][10]. The transmitting chain consists of a UWB pulse generator, a chirp FSK modulator, followed by a power amplifier, and an antenna. Depending on the transmitter binary information input, the chirp FSK modulator generates a dual-band FSK modulated signal by switching between two sub band signals [11]. The antenna emits the modulated signal once it has

been amplified by the power amplifier. The LNA is used to initially amplify the receiving signal. The input of a differential double-balanced down-conversion passive mixer is driven by the UWB RF differential LNA signal. The mixer switches are driven by four rectangular LO signals with a 25% duty-cycle LO wave tuned to 4 GHz. To separate the mixer's DC voltages from the LNA's and to obstruct the signals from the LNA's second-order intermodulation products, the mixer is linked to the LNA through an AC coupling capacitor. The mixer is loaded by a voltage amplifier and works in voltage mode. The bias of the mixer is set using resistors RB. A low pass filter (LPF) is often used to filter the voltage amplifier's output signal. The latter passes only the selected down-converted channel signal and suppresses the other channel. Finally, the chirp FSK demodulator will retrieve the digitally transmitted data[12] [13]. Given that the I and Q channels are active at the same time, the 50% duty cycle mixer suffers from IQ crosstalk and its effects on linearity and noise. Then, the Q channel loads the I channel, and vice versa. This phenomenon does not occur in the case of the 25% duty-cycle mixer, where only one channel is active at any given time.
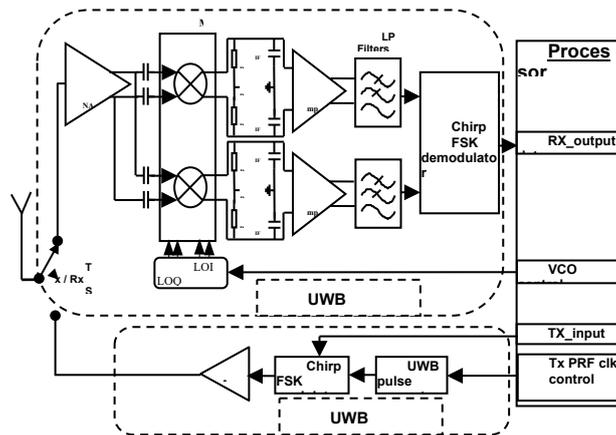

Fig. 1. Front-end topology of the UWB transceiver

The IQ crosstalk in a 25% duty-cycle mixer is much lower than in a 50% duty-cycle mixer. The CMOS passive mixer has good linearity and no DC power except for its clock generation circuit, and is less dependent on process variations, and has a smaller die area, and has better LO-RF feed through performance than an active mixer. Moreover, the LNA, LPF, and down-conversion passive mixer are designed differentially to reduce the second-order nonlinearity and cancel common-mode noise and interferences.

3   Mismatch analysis in LNA

3.1   LNA circuit

Figure 2 shows the Low Noise Amplifier circuit. It is based on the Balun topology that converts the single-ended input signal into a differential and uses a common gate stage (CG) (M1) and a common source stage (CS) (M2)[14]. The input impedance of this circuit is controlled by M1 transconductance (g_{m1}). When the gains of CS and CG are equivalent and in opposition to each other, the output noise is canceled [11]. The input impedance Z_{inCG} is given by:

$$Z_{inCG} = \frac{r_{oNmos} + r_{oPmos}}{r_{oNmos}(g_{m1} + g_{mb1}) + 1} \tag{1}$$

r_{oNmos} and r_{oPmos} are small signal output resistances for NMOS and PMOS transistors respectively.

Furthermore, distortion is decreased, allowing for the development of highly linear LNAs. If the CG-stage input impedance Z_{inCG} is equal to the source resistance R_s, the input impedance can be matched.

$$A_{LNA} = \frac{(V_{out}^+ - V_{out}^-)}{V_{in}} = A_{CG} - A_{CS} = 2g_{m1}\frac{r_{oNmos}\, r_{oPmos}}{r_{oNmos} + r_{oPmos}} \tag{2}$$

By tuning the DC voltage (V_{bias1}) at M_1 gate, we may change the current in M_2 and get an equal voltage gain at Vout+ and Vout-.

The DC voltage (V_{bias2}) is used to adjust LNA gain magnitude and NF by changing the output conductance of M3 and M4 respectively, that operate in the triode region.
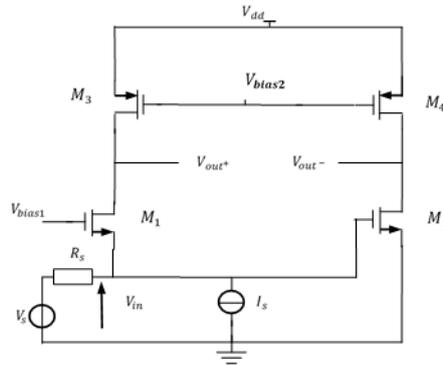

Fig. 2. Balun LNA

3.2   PMOS transistor mismatch model for the LNA

In the Triode area, an appropriate MOSFET model is:

$$I_D = \mu_P C_{ox} \frac{W}{L} (V_{SG} - V_{th}) V_{SD} \tag{3}$$

where I_D is the drain current, V_{SG} is the gate-source voltage, V_{th} is the threshold voltage, with C_{ox} being the gate-oxide capacitance per unit-area, μ_P as the carrier mobility, W and L being the width and length of the transistor respectively.

The objective of the following analysis is to find the value of the PMOS output offset voltage $V_o = V_{SD3} - V_{SD4}$ due to mismatches between transistors M3 and M4.

We pose $V_{th3} = V_{th}$ and $V_{th4} = V_{th} + \Delta V_{th}$.

we denote the ratio $\frac{W3}{L3} = Rat$ and $\frac{W4}{L4} = Rat + \Delta Rat$.

Mismatches in PMOS transistors lead to $I_{D3} \neq I_{D4}$.

We denote $I_{D3} = I_D$ and $I_{D4} = I_D + \Delta I_D$.

The currents can be approximated in the triode region (linear region) by:

$$I_{D3} = \mu_P C_{ox} \frac{W_3}{L_3} (V_{SG3} - V_{th3}) V_{SD3} \tag{4}$$

$$I_{D4} = \mu_P C_{ox} \frac{W_4}{L_4} (V_{SG4} - V_{th4}) V_{SD4} \tag{5}$$

In the following study we neglect $\mu_p C_{ox}$ *mismatch*. The output offset voltage is given by:

$$V_o = V_{SD3} - V_{SD4}$$
$$= \frac{I_D}{\mu_p C_{ox} Rat (V_{SG} - V_{th})} - \frac{I_D + \Delta I_D}{\mu_p C_{ox} (Rat + \Delta Rat)(V_{SG} - V_{th} - \Delta V_{th})}$$
$$= \frac{I_D}{\mu_p C_{ox} Rat (V_{SG} - V_{th})} \left[1 - \frac{1 + \frac{\Delta I_D}{I_D}}{(1 + \frac{\Delta Rat}{Rat})(1 - \frac{\Delta V_{th}}{V_{SG} - V_{th}})} \right] \tag{6}$$

$\frac{\Delta I_D}{I_D} \approx -\frac{\Delta Rd}{Rd}$

where Rd is the equivalent PMOS load for the differential delay circuit.

Assuming $\frac{\Delta Rat}{Rat} \ll 1$, $\frac{\Delta V_{th}}{V_{SG} - V_{th}} \ll 1$ and $\frac{\Delta I_D}{I_D} \ll 1$

equation (6) becomes:

$$V_o = \frac{I_D}{\mu_p C_{ox} Rat (V_{SG} - V_{th})} \left[\frac{\Delta Rat}{Rat} + \frac{\Delta Rd}{Rd} - \frac{\Delta V_{th}}{V_{SG} - V_{th}} \right] \tag{7}$$

$\frac{I_D}{\mu_p C_{ox} Rat (V_{SG} - V_{th})}$ is approximately equal to the equilibrium source drain voltage V_{SD} of each transistor. This gives:

$$V_o = V_{SD} \left[\frac{\Delta Rat}{Rat} + \frac{\Delta Rd}{Rd} - \frac{\Delta V_{th}}{V_{SG} - V_{th}} \right] \tag{8}$$

Equation (9) is an important result, revealing the dependence of V_o on device mismatches and bias conditions.

In order to produce high and stable LNA gain and cancel noise correctly we need to minimize $\frac{\Delta Rd}{Rd}, \frac{\Delta Rat}{Rat}, \Delta V_{th}$ and maximize $(V_{SG} - V_{th})$.

3.3 Simulation result for LNA

The most important flaws are PMOS transistor mismatches and random changes during differential LNA circuit manufacture. We are interested in determine how these incompatibilities affect gain, noise figure, and IIP2. The proposed design's robustness is studied by running a Monte Carlo simulation.

Also, we will evaluate the standard uncertainty given by the following equation:

$$\text{Standard uncertainty} = \text{Std uncertainty} = \text{Std. dev}/\sqrt{n} = \sqrt{\frac{1}{n(n-1)}\sum_{j=1}^{n}(x_j - \bar{x})^2} \tag{9}$$

where Std.dev is the Standard deviation given by:

$$Std.dev = \sqrt{\frac{1}{(n-1)}\sum_{j=1}^{n}(x_j - \bar{x})^2} \tag{10}$$

n is the number of observations, where $\bar{x}$ is the mean and x_j is the jth data point.

From statistical theory, 95% of the runs are in the range [mean - 2std uncertainty, mean + 2std uncertainty]. 95% is the level of confidence with a coverage factor of 2.

[mean - 2std uncertainty, mean + 2std uncertainty] is called confidence interval.

PMOS size mismatch. A number of Monte Carlo simulations were performed to demonstrate the impact of process modifications on the performance parameters of the LNA. The size of PMOS varied by 5% ($\frac{\Delta Rat}{Rat} = \pm 5\%$).

Figure 3(a) shows the Monte-Carlo simulation results of the LNA gain. As we see from the histogram data, the variation of $\frac{W}{L}$ value in PMOS transistors affects the gain, when $\frac{W}{L}$ changes by about 5%. From Figure 3 (a), we see that the mean of the LNA gain equals 30.15 dB and the standard uncertainty equals 0.0475 dB. These values are good for fabrication. 95% of the runs are in the range [30.055, 30.245]dB.

Figure 3(b) shows a gain variation of 25.46 dB to 21.5dB in the 3-5 GHz band, which is acceptable.

Figure 4 (a) shows the Monte Carlo simulation result for LNA NF in case of PMOS size mismatch the mean=3.146dB, std dev=0.368dB, std uncertainty=0.0184dB and relative uncertainty=0.58%. 95% of the runs are in the range [3.1092, 3.1828] dB. Figure 4 (b) shows NF vs. frequency.
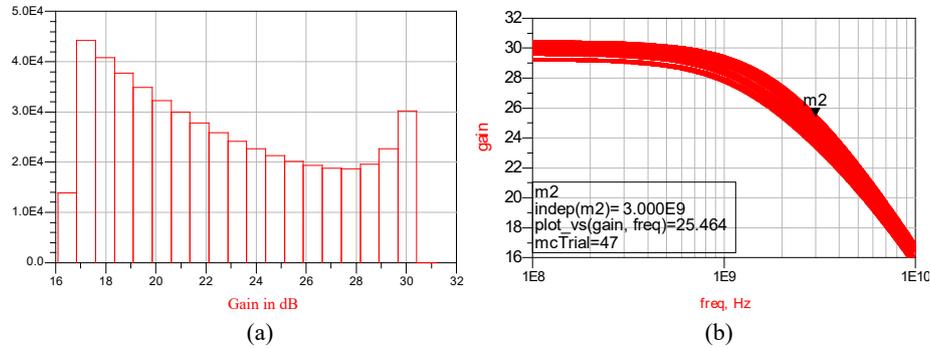
Fig. 3. LNA Gain for PMOS size mismatch a) Monte Carol simulation result, mean = 30.15 dB, std dev=0.336dB, std uncertainty=0.0475dB and relative uncertainty=0.157% b) LNA gain vs frequency
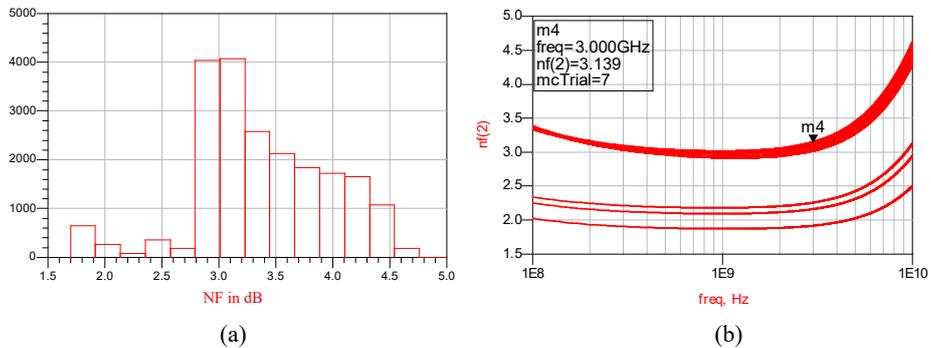

Fig. 4. LNA NF for PMOS size mismatch a) Monte Carol simulation result, mean=3.146dB, std dev=0.368dB, std uncertainty=0.0184dB and relative uncertainty=0.58% b) LNA NF vs frequency

The NF vary from 1.9dB to 3.4dB in the 3-5GHz band. The linearity performance is plotted in Figure 5.

In Figure 5 (a) Monte Carlo simulation result for LNA IIP2 is presented with a mean of 13.143dBm, a std dev equals to 3.34dBm, a std uncertainty of 0.472dBm and a relative uncertainty of 3.5%. Therefore the confidence interval of IIP2 is [12.199, 14.087]dBm.

Figure 5 (b) shows LNA IIP2 versus LNA input power Pin.

Therefore, the randomness of process due to PMOS size mismatch will affect the second order linearity but will not have a great impact on the gain and NF of the proposed LNA.
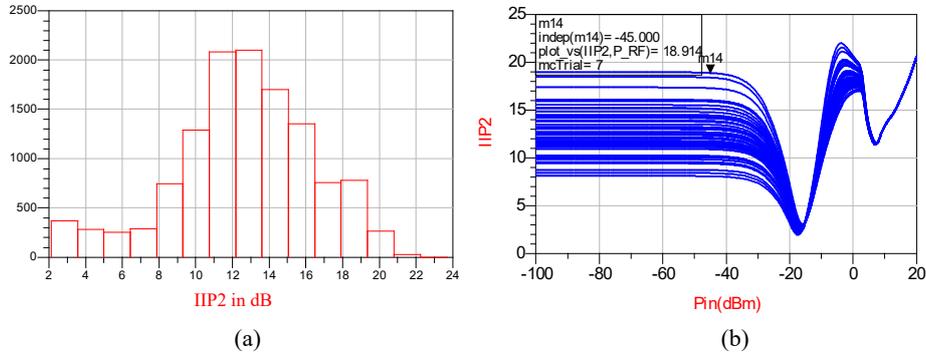
(a)   (b)

Fig. 5. LNA IIP2 for PMOS size mismatch a) Monte Carlo simulation result, mean=13.143 dBm, std dev=3.34dBm, std uncertainty=0.472dBm and relative uncertainty=3.5% b) LNA IIP2 vs Pin

PMOS Vth mismatch. In this part we will study the PMOS transistor voltage threshold (V_{th}) mismatch effect on the gain, NF, and IIP2.

The voltage threshold (V_{th}), was varied by 5% ($\frac{\Delta V_{th}}{V_{th}} = \pm 5\%$).

LNA Gain Monte Carlo analysis in Figure 6(a) shows mean=30.15dB, std dev=0.246dB, std uncertainty=0.0347dB, and relative uncertainty=0.11%. In Figure 6(b) we plot LNA Gain versus frequency for different Monte Carlo trials. The results found are very close to Figure 3. There is no significant PMOS V_{th} mismatch effect on gain. Therefore, ninety five percent of the observations of gain are in the range [30.0806, 30.2194] dB.

(a)   (b)

Fig. 6. LNA Gain for PMOS V_{th} mismatch a) Monte Carlo simulation result, mean=30.15dB ,std dev=0.246dB, std uncertainty=0.0347dB and relative uncertainty=0.11% b) LNA Gain vs frequency

Figure 7 depicts the corresponding NF in case of PMOS Vth mismatch. The mean equals to 3.176dB and the std dev equals to 0.001dB. Therefore, ninety five percent of the observations of NF are in the interval [3.17596, 3.17604]dB.

From Figure 7(b) the NF vary from 3.1dB to 3.32dB in the 3-5GHz band.

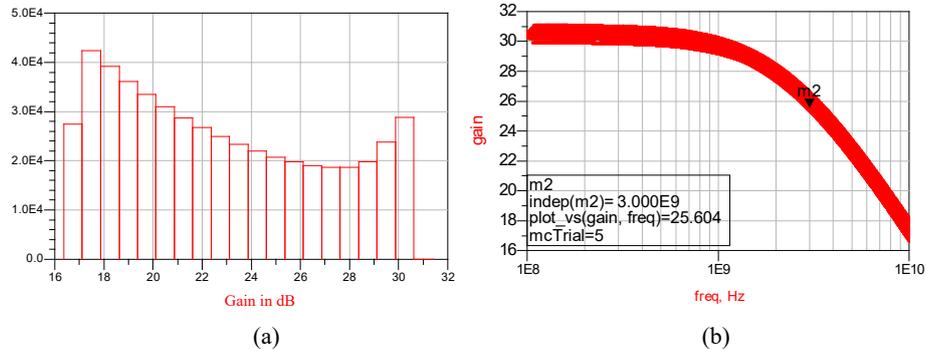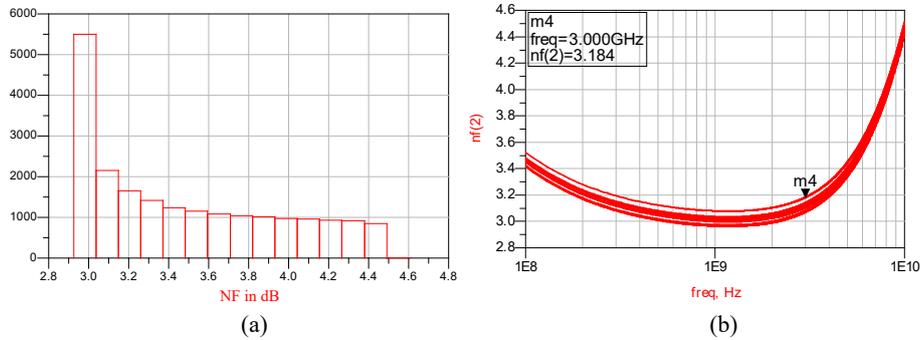(a)   (b)

Fig. 7. LNA NF for PMOS V_{th} mismatch a) Monte Carlo simulation result, mean=3.176dB, std dev=0.001dB, std uncertainty=0.00002dB and relative uncertainty=0.0007% b) LNA NF vs frequency

Monte Carlo simulation result for LNA IIP2 in case of PMOS Vth mismatch is depicted in Figure 8 (a) with a mean of 8.665dBm, the std dev=14.008dBm, the std uncertainty=1.98dBm and a relative uncertainty=22.8%. Figure 8 (b) shows LNA IIP2 versus input power.

Therefore the confidence interval of IIP2 is [4.705, 12.625]dBm.

Therefore, the PMOS V_{th} mismatch has a great influence on the second order intercept point of the LNA but will not have a significant impact on the gain and NF.

(a)   (b)

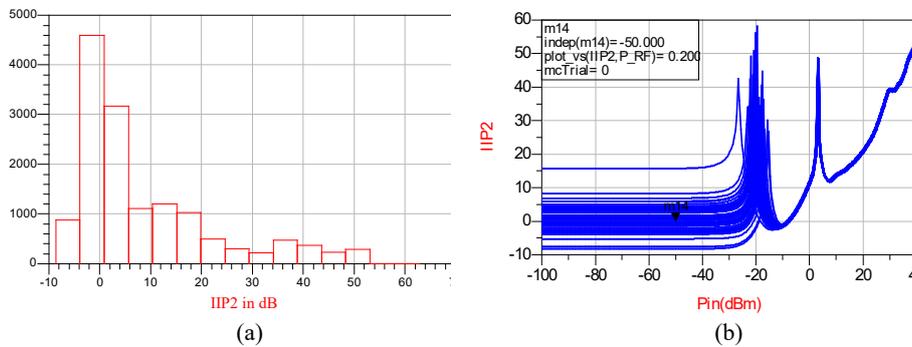**Fig. 8.** LNA IIP2 for PMOS V_{th} mismatch a) Monte Carlo simulation result, mean=8.665 dBm, std dev=14.008dBm, std uncertainty=1.98dBm and relative uncertainty=22.8% b) LNA IIP2 vs Pin

From this analysis, we can confirm that the LNA IIP2 is sensitive to the variation in the threshold voltage and size of PMOS transistors, but LNA Gain and NF are less sensitive. This is why care must be taken with the mismatch of PMOS transistors.

4   Mismatch analysis in the receiver front-end

4.1   Receiver front-end circuit

The passive mixer-based UWB receiver circuit is depicted in Figure 9. First, the LNA amplifies the UWB RF signal coming from the antenna. Then the differential RF signal VLNAout is down-converted by the 25% duty-cycle double-balanced passive mixer and appears through the baseband load ($C_{IF} \parallel R_B$). Due to their low power and improved linearity performance, 25% duty-cycle LO driven mixers have become quite popular recently [15][16]. To prevent the DC bias and the second-order intermodulation components produced inside the LNA, capacitors (C) are added to each mixer input.

Second-order intermodulation (IM2) products are mostly produced by the mixer during the overlap time when mixer switches operate concurrently [17] and [18]–[19], Asymmetric $\frac{W}{L}$ value or threshold voltage V_{th} in the NMOS switches of the mixer and unbalanced parasitic coupling between RF-to-LO or LO-to-RF ports cause IM2 products to be produced.

Additionally, due to their frequency dependant properties, the degree of the aforementioned mismatch effects grows as the operating frequency rises.

In the following, we study the effect of NMOS mixer switches mismatch on gain, NF, and IIP2 performance of the UWB receiver front end with a 25% duty cycle.

The NMOS switches nominal size is $\frac{w}{L} = \frac{17.8\mu m}{0.18\mu m}$.

Differential double-balanced down-conversion mixer

Fig. 9. Passive mixer-based UWB receiver circuit

The differential outputs of one channel do not overlap during the 25% duty-cycle LO-driven mixer, in contrast to a 50% duty-cycle LO-driven mixer. Although each channel should ideally receive an equal amount of RF current, random asymmetry considerations may result in improperly balanced switching operations [9].

Utilizing an offset voltage source (V_{os}) linked in series at the mixer switch's gate allows for the modeling of the V_{th} mismatch.

4.2 NMOS transistor mismatch model for the mixer

The NMOS transistors of the passive mixer work as switches. This means that they operate in the linear region of the triode area, an appropriate NMOS current model in this region is given by:

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})V_{DS} \qquad \text{for} \quad V_{DS} \ll (V_{GS} - V_{th}) \tag{11}$$

where I_D is the drain current, $(V_{GS} - V_{th})$ is the overdrive voltage, V_{th} is the threshold voltage, with C_{ox} being the gate-oxide capacitance per unit-area, μ_n as the carrier mobility, W and L being the width and length of the transistor respectively. $\frac{W}{L}$ is the aspect ratio.

The drain current is a linear function of V_{DS}, this implies that the resistance between source and drain can be controlled by the overdrive voltage.

We will study random mismatch between tow NMOS transistors in the mixer circuit. Suppose that the drain current are denoted I_{D1} and I_{D2}:

$$I_{D1} = \mu_n C_{ox}(\frac{W}{L})_1(V_{GS} - V_{th1})V_{DS1} \tag{12}$$

$$I_{D2} = \mu_n C_{ox}(\frac{W}{L})_2(V_{GS} - V_{th2})V_{DS2} \tag{13}$$

The current offset $\Delta I_D = I_{D1} - I_{D2}$ and the nominal current $I_D = \frac{I_{D1}+I_{D2}}{2}$

The size offset $\Delta(\frac{W}{L}) = (\frac{W}{L})_1 - (\frac{W}{L})_2$ and the nominal size $\frac{W}{L} = \frac{(\frac{W}{L})_1+(\frac{W}{L})_2}{2}$

The threshold voltage offset $\Delta V_{th} = V_{th1} - V_{th2}$ and the nominal threshold voltage $V_{th} = \frac{V_{th1}-V_{th2}}{2}$

Assuming $V_{DS1} \approx V_{DS2}$ and mismatches in $\mu_n C_{ox}$ is neglected, it follows:

$$\frac{\Delta I_D}{I_D} = \frac{V_{GS}}{V_{GS}-V_{th}}\frac{\Delta(\frac{W}{L})}{\frac{W}{L}} - \frac{\Delta V_{th}}{V_{GS}-V_{th}} \tag{14}$$

$\frac{\Delta I_D}{I_D}$ depends on the aspect ratio mismatch, the threshold voltage mismatch and the overdrive voltage mismatch.

This result suggests that, to minimize NMOS current mismatch, and thus reducing IM2 products, the overdrive voltage must be maximized. This is done when we have run simulation on the receiver front end using ADS tool.

4.3 Simulation result for the receiver front-end

Mixer NMOS switches size mismatch. A Monte Carlo simulations were run to evaluate the impact of process modifications on the performance parameters of the receiver front end. The size of mixer NMOS switches was varied by 5% from its nominal value ($\Delta(\frac{W}{L}) = \pm 5\%$)

Figure 10 shows Monte Carlo simulation result of IIP2 for the receiver front end. The mean=24.722dBm, the std dev=0.54dBm, the std uncertainty=0.024dBm and relative uncertainty=0.097%.

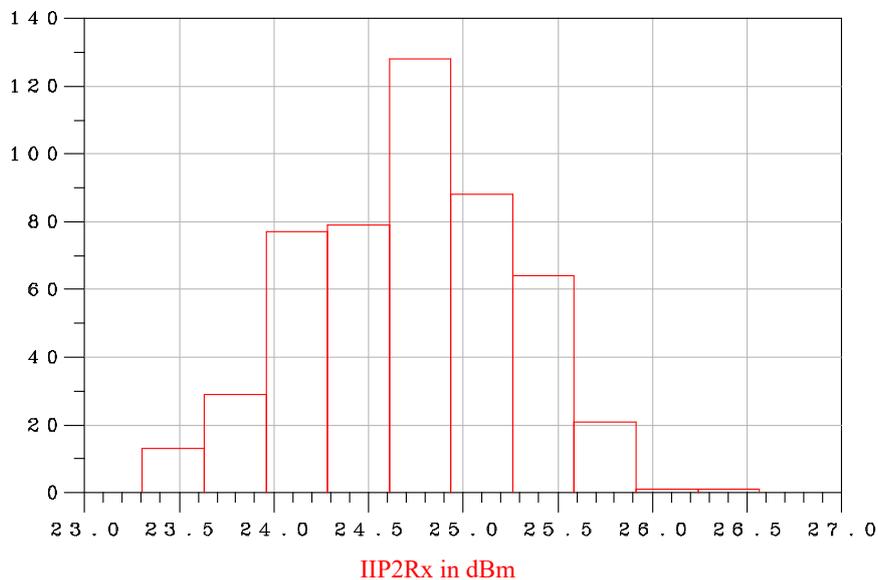Therefore the confidence interval of receiver IIP2 is [24.674, 24.77]dBm.

Fig. 10. IIP2Rx Monte Carlo simulation result for Mixer NMOS size mismatch, mean=24.722 dBm, std dev=0.54dBm, std uncertainty=0.024dBm and relative uncertainty=0.097%

As we see in Figure 11(a) from Monte-Carlo simulation data, the mixer NMOS size mismatch of $\pm 5\%$ affects the receiver front end gain. The results show that the mean of GainRx equals 15.285dB and the standard deviation (std dev) =2.081dB for a frequency of 4 GHz.

Figure 11 (b) shows GainRx versus input power Pin for different Monte-Carlo trials. A 95% of receiver gain trials are in the range [15.099, 15.471] dB.
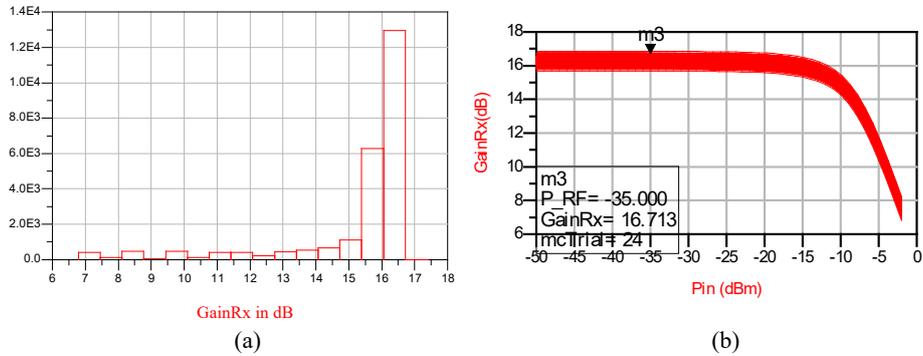
(a)   (b)

Fig. 11. GainRx for Mixer NMOS size mismatch a) Monte Carlo simulation result, mean = 15.285dB, std dev=2.081dB, std uncertainty=0.093dB and relative uncertainty=0.6% b) GainRx vs Pin

Mixer NMOS switches Vth mismatch. In this part, we will study the voltage threshold (V_{th}) mismatch effect on the receiver's front end performance. The voltage threshold (V_{th}), was varied by 5% ($\frac{\Delta V_{th}}{V_{th}} = \pm 5\%$). The Monte Carlo simulation result for the receiver IIP2 in the case of a NMOS Vth mismatch is depicted in Figure 12 with 500 iterations. We get a mean of 24.758dBm, the std dev=1.107dBm, and a relative uncertainty=0.2%. Therefore 95% of receiver IIP2 trials are in the range [24.659, 24.857] dBm.
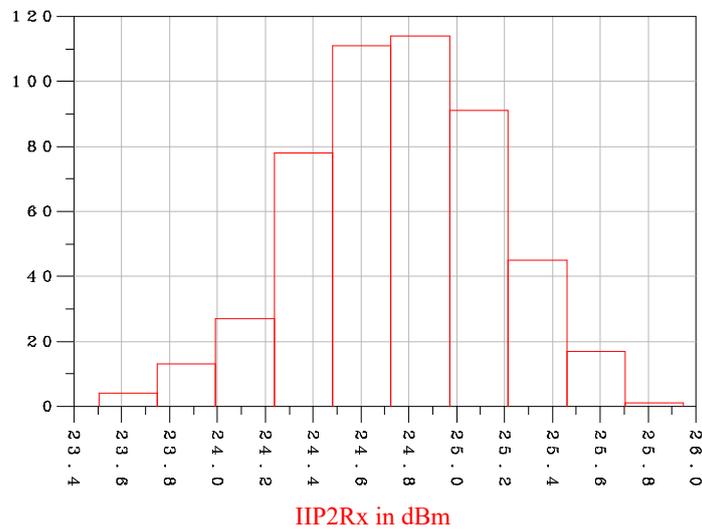

Fig. 12. IIP2Rx Monte Carlo simulation result for Mixer NMOS V_{th} mismatch, mean=24.758 dBm, std dev=1.107dBm, std uncertainty=0.0495dBm and relative uncertainty=0.2%

In Figure 13(a), we see Monte-Carlo simulation results for GainRx, in the case of mixer NMOS V_{th} mismatch of $\pm 5\%$. The results show that the mean of GainRx equals 10.709 dB and the standard deviation (std dev)=2.246 dB.

Figure 13 (b), shows GainRx versus input power Pin for different Monte-Carlo trials. A 95% of receiver Gain trials are in the confidence interval [10.509, 10.909] dB.
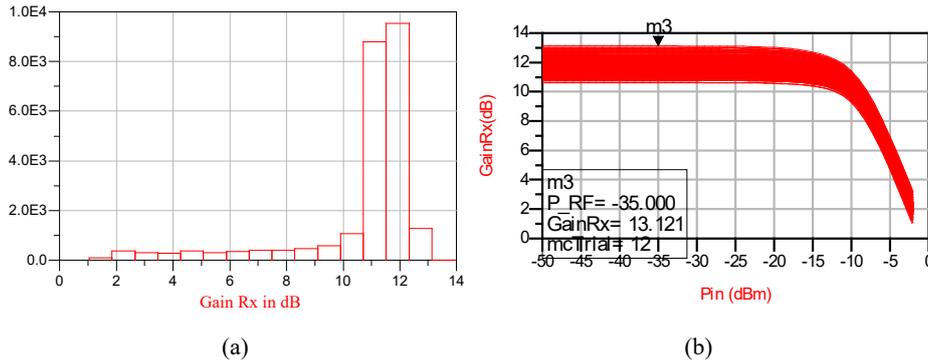

| (a) | (b) |

Fig. 13. GainRx for Mixer NMOS V_{th} mismatch a) Monte Carlo simulation result, mean= 10.709dB, std dev=2.246dB, std uncertainty=0.1dB and relative uncertainty=0.93% b) GainRx vs Pin

Table 1 summarizes Gain and IIP2 for LNA and Receiver front-end with the corresponding confidence interval at 95% of confidence.

Table 1. Summary of Gain and IIP2 for LNA and Receiver front-end

	LNA		Receiver front-end	
	PMOS $\frac{W}{L}$ mismatch	**PMOS V_{th} mismatch**	**NMOS switches $\frac{W}{L}$ mismatch**	**NMOS switches V_{th} mismatch**
Mean Gain(dB)	30.15	30.15	15.285	10.709
Gain confidence interval(dB)	[30.055, 30.245]	[30.0806, 30.2194]	[15.099, 15.471]	[10.509, 10.909]
Mean IIP2(dBm)	13.143	8.665	24.722	24.758
IIP2 confidence interval(dBm)	[12.199, 14.087]	[4.705, 12.625]	[24.674, 24.77]	[24.659, 24.857]

5   Conclusion

The impact of device mismatches on differential UWB receivers front end performances were examined in this research. Two transistor mismatch models was proposed in order to evaluate the LNA output offset voltage and mixer offset current. A number of Monte Carlo simulations were performed in order to analyze the impact of a random variation in PMOS $\frac{W}{L}$ and voltage threshold on LNA gain, NF, and IIP2. It is shown that the LNA IIP2 is sensitive to the variation in the threshold voltage and size

of PMOS transistors but the LNA Gain and NF are less sensitive. A Monte Carlo and harmonic balance simulation were run to evaluate the impact of process modifications on the performance parameters of the receiver front-end. The size of mixer NMOS switches was varied by 5% from its nominal value. Simulation results show that IIP2 of the receiver is not very sensitive to mixer NMOS mismatches. The receiver IIP2 confidence interval is [24.674, 24.77] dBm for NMOS switches $\frac{W}{L}$ mismatch and [24.659, 24.857] dBm for NMOS switch V_{th} mismatch. This shows no significant behavioral variations in the receiver's front end linearity performance. Therefore, the proposed UWB receiver front end circuit meets UWB specifications perfectly, which makes it a good candidate for WBAN applications.

6 References

[1] K. Hasan, K. Biswas, K. Ahmed, N. S. Nafi, and M. S. Islam, "A comprehensive review of wireless body area network," *J. Netw. Comput. Appl.*, vol. 143, pp. 178–198, 2019. https://doi.org/10.1016/j.jnca.2019.06.016

[2] S. Movassaghi, M. Abolhasan, J. Lipman, D. Smith, and A. Jamalipour, "Wireless body area networks: A survey," *IEEE Commun. Surv. tutorials*, vol. 16, no. 3, pp. 1658–1686, 2014. https://doi.org/10.1109/SURV.2013.121313.00064

[3] S. Al-Janabi, I. Al-Shourbaji, M. Shojafar, and S. Shamshirband, "Survey of main challenges (security and privacy) in wireless body area networks for healthcare applications," *Egypt. Informatics J.*, vol. 18, no. 2, pp. 113–122, 2017. https://doi.org/10.1016/j.eij.2016.11.001

[4] B. Razavi, *Design of analog CMOS integrated circuits*. 清华大学出版社有限公司, 2005.

[5] T. Serrano-Gotarredona and B. Linares-Barranco, "A new five-parameter MOS transistor mismatch model," *IEEE Electron Device Lett.*, vol. 21, no. 1, pp. 37–39, 2000. https://doi.org/10.1109/55.817445

[6] P. G. Drennan and C. C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 450–456, 2003. https://doi.org/10.1109/JSSC.2002.808305

[7] J. Wang and A. K. K. Wong, "Effects of mismatch on CMOS double-balanced mixers: a theoretical analysis," in *Proceedings 2001 IEEE Hong Kong Electron Devices Meeting (Cat. No. 01TH8553)*, 2001, pp. 85–88.

[8] D. Bhatt, J. Mukherjee, and J.-M. Redouté, "A Self-Biased Mixer in $0.18\mu\text{m}$ CMOS for an Ultra-Wideband Receiver," *IEEE Trans. Microw. Theory Tech.*, vol. 65, no. 4, pp. 1294–1302, 2017. https://doi.org/10.1109/TMTT.2016.2640949

[9] J. Han and K. Kwon, "RF receiver front-end employing IIP2-enhanced 25% duty-cycle quadrature passive mixer for advanced cellular applications," *IEEE Access*, vol. 8, pp. 8166–8177, 2020. https://doi.org/10.1109/ACCESS.2020.2964651

[10] K. R. Laker and W. M. C. Sansen, *Design of analog integrated circuits and systems*, vol. 1. McGraw-Hill New York, 1994.

[11] T. A. Kareem and H. Trabelsi, "A Novel CSS-UWB Receiver Front-End," in *2022 IEEE International Conference on Design & Test of Integrated Micro & Nano-Systems (DTS)*, 2022, pp. 1–5. https://doi.org/10.1109/DTS55284.2022.9809853

[12] T. A. Kareem and H. Trabelsi, "A Broadband High Gain, Noise-Canceling Balun LNA with 3–5 GHz UWB Receivers for Medical Applications.," *Int. J. Online Biomed. Eng.*, vol. 18, no. 3, 2022. https://doi.org/10.3991/ijoe.v18i03.28009

[13] H. Trabelsi, I. Barraj, and M. Masmoudi, "A 3–5 GHz FSK-UWB transmitter for wireless personal healthcare applications," *AEU-International J. Electron. Commun.*, vol. 69, no. 1, pp. 262–273, 2015. https://doi.org/10.1016/j.aeue.2014.09.009

[14] Q. M. Abubaker and L. Albasha, "Balun LNA thermal noise analysis and balancing with common-source degeneration resistor," *IEEE Access*, vol. 8, pp. 64949–64958, 2020. https://doi.org/10.1109/ACCESS.2020.2984314

[15] D. Kaczman *et al.*, "A Single–Chip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-less CMOS Receiver With DigRF 3G Interface and ${+}$ $90 dBm IIP2," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 718–739, 2009. https://doi.org/10.1109/JSSC.2009.2013–762

[16] A. Mirzaei, H. Darabi, J. C. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 57, no. 9, pp. 2353–2366, 2010. https://doi.org/10.1109/TCSI.2010.2043014

[17] J. Han and K. Kwon, "A SAW-less receiver front-end employing body-effect control IIP2 calibration," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 61, no. 9, pp. 2691–2698, 2014. https://doi.org/10.1109/TCSI.2014.2332260

[18] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order intermodulation mechanisms in CMOS downconverters," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394–406, 2003. https://doi.org/10.1109/JSSC.2002.808310

[19] S. Chehrazi, A. Mirzaei, and A. A. Abidi, "Second-order intermodulation in current-commutating passive FET mixers," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 56, no. 12, pp. 2556–2568, 2009. https://doi.org/10.1109/TCSI.2009.2016630

[20] M. K. Jabbar and H. Trabelsi, "Clustering Review in Vehicular Ad hoc Networks: Algorithms, Comparisons, Challenges and Solutions.," *Int. J. Interact. Mob. Technol.*, vol. 16, no. 10, 2022. https://doi.org/10.3991/ijim.v16i10.29973

[21] T. Kareem, M. A. Hussain, and M. K. Jabbar, "Particle Swarm Optimization Based Beamforming in Massive MIMO Systems," 2020. https://doi.org/10.3991/ijim.v14i05.13701

[22] H. Hazim, H. Al-Behadili, T. Kareem, and M. Jabbar, "Design of mobile communication system for emergency services," 2020. https://doi.org/10.3991/ijim.v14i13.14623

7 Authors

Thaar A. Kareem is a lecturer in Electric Engineering Department - College of Engineering, University of Misan, Iraq. He obtained BSC from university of Baghdad, Iraq and the master from EMU, north Cyprus. Now he is a PhD student in Systems Integration & Emerging Energies Laboratory, Electrical Engineering Department, National Engineers School of Sfax, University of Sfax B.P. 1173, Sfax 3038, Tunisia (E-mail: thaar_kareem@uomisan.edu.iq).

Saif Benali was born in Tunisia in 1991.He received the License in science and technology of information and communication from the Higher Institute of Electronics and Communication of Sfax, Tunisia in 2013, the Master degree in telecommunications and network systems in 2015 from the National School of Electronics and Telecommunications of Sfax, Tunisia and the PhD in electrical engineering in 2022 from the National Engineering School of Gabes, Tunisia. He joined the Systems Integration & Emerging Energies laboratory (SI2E) at the National Engineering School

of Sfax, Tunisia since 2016. His current field of research is in radio architectures and design of Analog CMOS RF integrated circuits for Ultra WideBand transceivers (E-mail: saifbenali.enet@gmail.com).

Hatem Trabelsi was born in Sfax, Tunisia in 1969. He received the engineering degree in electrical engineering from the National School of Engineers of Tunis in 1993, the aggregation degree in 2001, Ph.D. in electrical engineering in 2009 and HDR in electrical engineering from the National School of Engineers of Sfax in 2015. His research was mainly focused on Microelectronic circuit design and implementation of ultra low power transceivers for Wireless Sensor Network. He is a member of the research laboratory Systems Integration & Emerging Energies Laboratory (SI2E), ENIS, where he is working in the field of analog and RF circuit design for ultra-wideband systems. His research interests are single-chip CMOS transceivers, RF front-ends, Ultra wideband analog circuit design. He is the author and co-author of several papers in the Microelectronic field. He is currently a Professor at the Electrical Engineering Department of the National School of Engineers of Sfax, University of Sfax B.P. 1173, Sfax 3038, Tunisia (E-mail: hatem.trabelsi@enis.tn).