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# Optimal Controller Design and Dynamic Performance Enhancement of High Step-up Non-Isolated DC-DC Converter for Electric Vehicle Charging Applications

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**Abstract** – *Ideally, traditional boost converters can achieve a high conversion ratio with a high-duty cycle. But, in regular practice, due to low conversion efficiency, RR reverse-recovery, and EMI (electromagnetic interference) problems, the high voltage gain cannot be performed, whereas CIBC (coupled inductor-based converters) can achieve high voltage gain by re-adjusting the turn ratios. Even though the leakage inductor of the CI (coupled inductor) makes some problems like voltage spikes on the main connectivity switch, high power dissipation, and voltage pressure can be minimized by voltage clamp. In this paper, a non-isolated DC-DC converter with high voltage gain is demonstrated with 3 diodes, 3 capacitors, 1-inductor, and a coupled inductor. The main inductor is connected to the input to decrease the current ripple. The voltage stress at main switch S is shared by diode $D_1$ and capacitor $C_1$ and the main switch is turned ON under zero current, hence it turns to low switching losses. This paper proposes two controllers like proportional-integral (PI) controller and fuzzy logic (FLC) for dc-dc converter. Furthermore, it demonstrates the operation, design, mathematical analysis, and performance of DC-DC converter using controllers for efficient operation of the system is performed using simulations in MATLAB 2012b.*

***Keywords***: *EV, Electric Vehicles, proportional integral, PI, On-Board Charger, fuzzy logic, FL, DC-DC*

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## I. Introduction

Generally, environmental problems are caused by using non-renewable energy resources like fossil fuels, coal energies, etc. So by using PV, wind, and Tidal energy the environmental problems are reduced. This energy's applied at the input side or Distribution generation (DG) systems. Due to the climatic effects the voltage gain will be reduced [1-3]. It's the major drawback of using renewable energy sources. Moreover, it's an effective method, by using PV panels the number of PV cells is connected in series so that output voltage across the PV panel will be improved. A dark effect cannot be obtained [4-5]. The main advantages are a large transmission ratio, excessive voltage gain, and small size [6-8]. Input current ripples are the main consideration by using photo voltaic and fuel cell applications. Moreover, similar advantages are getting by using an ideal converter but during the practical conditions due to less Transmission efficiency, reverse recovery, and EMI problems high voltage gain will not achieve [9-10], [28]. However, many converters with different new techniques have been introduced for getting high voltage gain and high transmission efficiency [11], [24].

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Switched capacitors [11-13] and voltage lift techniques [14-16] have been introduced for improving the voltage gain. High current ripples at the input side are the main disadvantage so it reduces the performance and efficiency of the converter. Recently there are many non-isolated coupled inductors-based converter are presented with different voltage clamping circuits [19-25]. They have the merit of high voltage gain; recovery of the leakage inductor's energy and low switching voltage stress are the main features and have the main drawback of high input current ripple. This makes problems in tracking the maximum power point (MPP) of PV panels.

The proposed converter Figure 1 has excessive voltage gain by maintaining the required turn ratio. Moreover, using a Leakage inductor across the coupled inductor [17-19] produces voltage spikes across the main switch so it leads to more power discharge. By providing voltage clamping circuits the power stored in the leakage inductor will be recovered. So, it's very important to provide voltage clamping circuits across the main switch S.

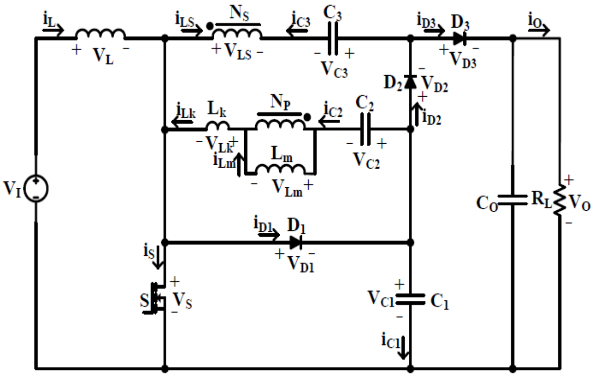

Figure. 1. Schematic of Non-Isolated DC-DC converter

The inductor is connected in series to the input side for minimizing the ripple currents at the input side. The voltage stress across switch S is shared by diode $D_1$ and capacitor $C_1$ and the main switch is turned on under zero current switching and conduction losses also decreased.

## II. Operating principle and Analysis

Operating principle and analysis, consider to 1) all capacitors C and inductors L & $L_m$ are taken large beyond any ripple voltages and currents, 2) Only leakage inductance $I_{LK}$ is considered.

### *II.1.* CCM Analysis of the non-isolated dc-dc Converter

It consists of 5 time intervals in a single switching period. Figure. II to Figure. VII shows a flow of the current path in CCM mode. The $N_S$ current of the non-isolated coupled inductor is:

$$i_{LS}=\frac{i_{Lm}-i_{Lk}}{n} \tag{1}$$

There is no simultaneous change in $i_L$ & $i_{LS}$, the study state performance is given below.

**Mode I [$t_0$<t<$t_1$]:** S and $D_3$ are in conduction. In this period iLk is increased & equal to $_{iLm.}$ This mode of operation ends when $I_{LK}$ equals $I_{LM}$.

The equation of $i_{LK}$,

$$i_{Lk}=\frac{1}{L_K}\int_{t_0}^{t_1}\left(V_{C1}-V_{C2}+\frac{V_0-V_{C3}}{n}\right)dt \tag{2}$$

The operating period of this mode is very small, where the value of $L_K$ is less and $V_{LK}$ is high. L becomes magnetized due to $V_1$, ending of this first mode, $I_{D3}$ becomes zero due to the secondary current of the inductor. Using KCL, $I_S$ can take as

$$i_s=i_L+i_{Lk}-i_{Ls} \tag{3}$$

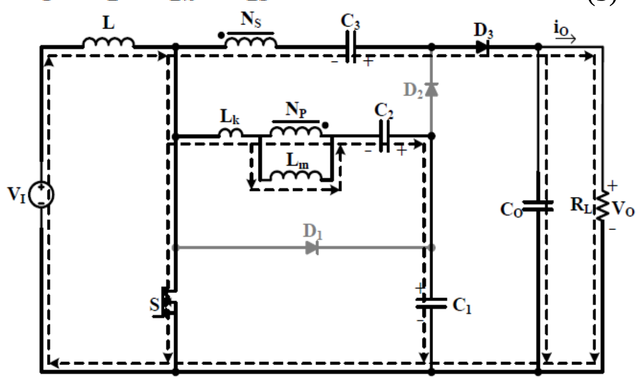

Figure 2. First Mode of Interval [$t_o$-$t_1$]

**Mode II [$t_1$<t<$t_2$]:** In this period the switch is still ON. The $i_{LK}$ improved and became more than then $i_{LM}$. The $i_{LK}$ equation is written as follows:

$$V_{Lk2}=\frac{\left(i_{Lk(t2)}-i_{Lk(t1)}\right)}{DT_S}L_K,\ i_{Lk}=ni_{D2}+i_{Lm} \tag{4}$$

$D_2$ ON due to $N_S$ current. Thus, the $D_2$ current improved from zero. Due to $N_S$ current, the $C_3$ is charged .$C_1$ energy is discharged through the coupled inductor and $C_2$. L is energized because of $V_1$. This period ends when S is OFF Using KVL the equations can be written as:

$$V_L=V_1 \tag{5}$$

$$V_{Lm}=V_{C2}-V_{C1}-V_{Lk2} \tag{6}$$

$$V_{C3}=(n+1)V_{C1}-nV_{C2}-nV_{Lk2} \tag{7}$$

Figure 3 shows the second mode of the interval [t1-t2]. Where n is the turns ratio of coupled inductor = $N_S$/$N_P$

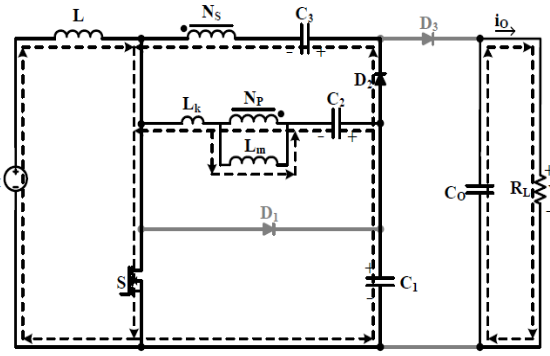

Figure 3. Second mode of interval [$t_1$-$t_2$]

**Mode III [$t_2<t<t_3$]:** switch S is OFF, $i_L$ current flows through $D_1$ and makes it conduction. $D_1$ and $D_2$ currents are written as:

$$i_{D1} = i_L + i_{Lk} + i_{D2} \quad (8)$$

$$i_{D2} = \frac{i_{Lk} - i_{Lm}}{n} \quad (9)$$

The $i_{Lk}$ is de-energized continuously until its equals the $i_{Lm}$. At this time $i_{D2}$ becomes zero.
$i_{LK}$ can be expressed as follows:

$$i_{Lk} = \frac{1}{L_k}\int_{t_0}^{t_1}\left(\frac{V_{C3}}{n} - V_{C2}\right)dt \quad (10)$$

According to the above equation, less value of leakage inductor and high –ve voltage causes a high current slope. Operating time is also small in this mode. Due to the de-energizing of inductors L and $V_1$ the $C_1$ is charged. This mode is when $D_2$ OFF. Figure 4 shows the Third mode of the interval [t2-t3]

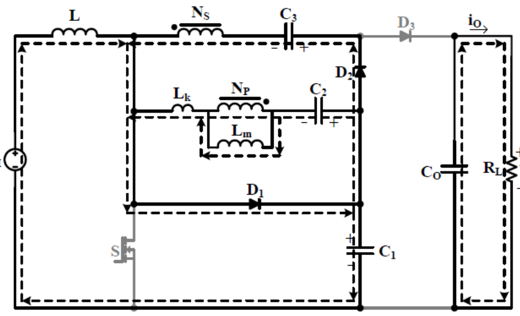

Figure 4. Third mode of the interval [$t_2$-$t_3$]

**Mode IV [$t_3<t<t_4$]:** The $C_1$ is charged by $V_1$ and storage energy in L. the leakage inductor voltage becomes charged in this mode. Its voltage is written as follows:

$$V_{Lk4} = \frac{\left(i_{Lk(t4)} - i_{Lk(t3)}\right)}{d_4 T_S} L_K,\ i_{Lk} = -n i_{D3} + i_{Lm} \quad (11)$$

Where $d_4T_S$ is the time interval of this period. $C_0$ is energized due to $N_S$ current. $D_1$ current will be written as:

$$i_{D1} = i_L + i_{Lm} - (n+1) i_{D3} \quad (12)$$

This period ends when $D_1$ current becomes zero. However, the slope of $i_{Lm}$ is less than $i_{LK}$, according to equation (1), the slop $i_{D3}$ is +ve. In this mode the $V_L$, $V_{Lm}$, can be expressed as:

$$V_L = V_1 - V_{C1} \quad (13)$$

$$V_{Lm} = -V_{C1} - V_{Lk4} \quad (14)$$

$$V_{Lm} = V_{C1} + V_{C3} + nV_{C2} + nV_{Lk4} \quad (15)$$

Figure 5 shows the fourth mode of the interval [t3-t4].

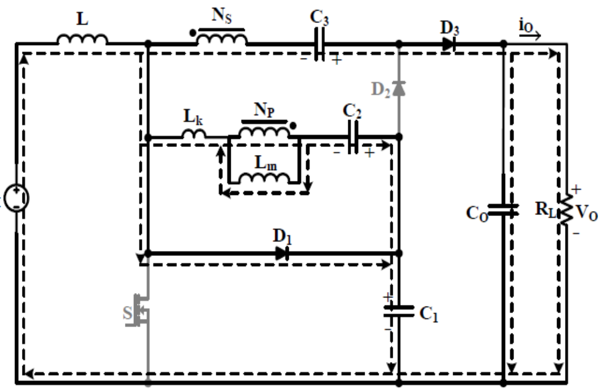

Figure 5. Fourth mode of the interval [$t_3$-$t_4$]

**Mode V [$t_4<t<t_5$]:** $D_3$ is still conducting in this period. Due to $i_{D3}$, the $C_0$ is energized. The $i_{D3}$ is expressed as:

$$i_{D3} = \frac{i_L + i_{Lm}}{n+1},\ i_{Lk} = \frac{-n}{n+1}\left(i_L - \frac{i_{Lm}}{n}\right) \quad (16)$$

The diode $D_3$ and the $i_{LK}$ slope calculate on the $i_L$, $i_{Lm}$ slope. Eliminating the $i_L$, $i_{Lm}$ ripples take the slope of $i_{D3}$ and the $i_{LK}$ tends to zero. Then $V_{Lk}$ will become zero. As in this equation, zero currents are possible when S becomes conduction like the beginning mode. In ZCS condition the switch is off. From KVL the voltage equation is written as:

$$V_{Lm} = -V_{C2} - \frac{n}{n+1} V_{Lk4} - \frac{V_{Lk5}}{n+1} \quad (17)$$

$$V_L = V_1 - V_{C1} - \frac{n}{n+1}\left(V_{Lk4} - V_{Lk5}\right) \quad (18)$$

$V_{LK2}$ & $V_{LK4}$ calculated from the $i_{Lk}$ slope in periods II &IV. $C_2$ and $C_3$ are in series with NS and NP, $i_{Lk}$ and $i_{Lm}$ avg. currents are zero, according to Amp-Sec balance law. Considering the balancing law in $C_1$, $C_2$ &$C_3$, and $C_0$ it can be justified that the average value of the diode current is equal to the $i_o$. So, the following equation can be obtained from Figure 2,

$$\langle i_{D2} \rangle = I_0 \Rightarrow D i_{D2\,peak} = 2I_0 \Rightarrow i_{D2\,peak} = \frac{2I_0}{D} \quad (19)$$

$$\frac{i_{Lk}-i_{Lm}}{n} = i_{D2\,peak} = \frac{2I_0}{D} \Rightarrow i_{Lk\,peak} = \frac{2nI_0}{D} \quad (20)$$

So, the ripples of the L & $L_m$ are also not considered in the $V_{gain}$ calculation. The $i_{stress}$ of the S and $D_1$ can be getting as given below:

$$i_{D1peak} = i_L + i_{Lm} + (n+1)i_{D2peak} = \left(\frac{2n+2-nD}{D(1-D)}\right) I_0 \quad (21)$$

By not considering the 3rd mode using this equation, the 4th time interval can be obtained as

$$\langle i_{D1} \rangle = I_0 = \frac{d_4 T_S I_L}{2T_S} \Rightarrow d_4 = \frac{2(1-D)}{n+2} \quad (22)$$

Due to (4) and (19) equations the voltage $V_{Lk2}$ can be found as:

$$V_{Lk2} = \frac{2nV_0}{D^2} Q, Q = \frac{f_S L_K}{R_L} \quad (23)$$

Where, $f_{switch}$ and $R_L$, respectively. Join Volt-Sec balance basis on the $L_K$ by neglecting modes 1&3, the following equation is obtained.

$$DT_S V_{LK2} + d_4 T_S V_{LK4} + 0 = 0 \Rightarrow V_{LK2} = -\frac{d_4}{D} V_{Lk4} \quad (24)$$

Applying Volt-Sec balance basis on the inductors the output is:

$$V_{C1} = \frac{V_1}{(1-D)} - \frac{n^2}{(n+1)(n+2)} V_{Lk4} \quad (25)$$

$$V_{C2} = \frac{DV_1}{(1-D)} - \frac{n^2}{(n+1)(n+2)} V_{Lk4} \quad (26)$$

$$V_{C3} = \frac{1+n-nD}{(1-D)} V_1 - \frac{n^2}{(n+1)(n+2)} V_{Lk4} - nV_{Lk2} \quad (27)$$

$$M = \frac{(n+1)(1-D)D^2}{(n+1)(1+D)D^2 - n^2(-2(1+n)+nD) \times Q} \left[\frac{2+n}{1-D}\right] \quad (28)$$

As the above expression depends on switching frequency, RL, and ILK value the voltage gain of this new converter is controlled. Whatever, it does not contain significant change on the Vgain. The change of Q on the voltage gain is shown in Fig IV and it's nearly low. For example, $f_S$=30 KHz, $L_K$=5uH, $R_L$=200 & D=0.5, the $Q_{factor}$ value is about 0.96.

The actual $V_{gain}$ is 96% of the conventional $V_{gain}$. The $V_{gain}$ of the new converter is

$$M_{CCM} = \frac{2+n}{1-D} \quad (29)$$

Figure 6 shows the fifth mode of the interval [$t_5$-$t_6$] and Figure 7 presents the current waveforms for the new converter in CCM Mode.

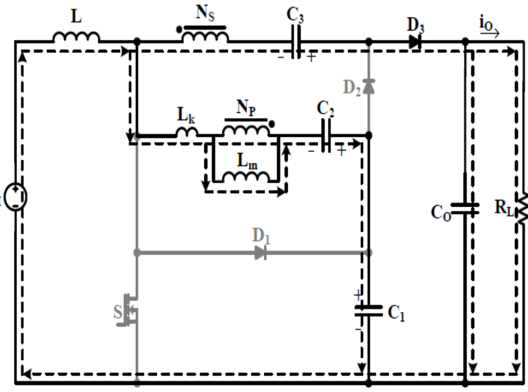


Figure 6. Fifth mode of the interval [$t_5$-$t_6$]

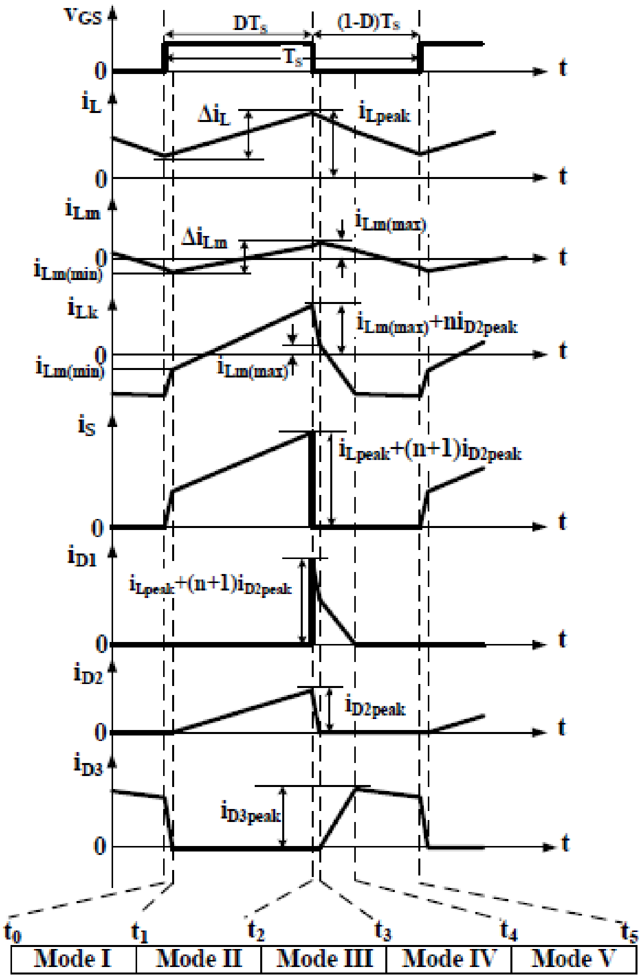


Figure 7. Current waveforms for new converter in CCM Mode

## B. Boundary Condition Mode (BCM)

In this mode, at ending of the switching period currents of L and $L_m$ become equal. Equations can be written as follows

$$i_{L\,min} = -i_{Lm\,min} \quad (30)$$

$$i_L(DT_S) = i_L(0) + \frac{1}{L}\int_0^{DT_S} V_1 dt \Rightarrow \Delta i_L = \frac{DV_1}{Lf_s} \quad (31)$$

$$i_{Lm}(DT_S) = i_{Lm}(0) + \frac{1}{Lm}\int_0^{DT_S} V_1 dt \Rightarrow \Delta i_{Lm} = \frac{DV_1}{L_m f_S} \quad (32)$$

Operating CCM mode in the new converter, coupled inductor Lm should be in CCM. Since $N_S$ and $N_P$ of the coupled inductor are series to the $C_2$ and $C_3$ according to the Amp-Sec balance Law, avg $i_{LK}$ & $i_{LM}$ is zero. At the end of this switching period, $D_3$ current reaches zero in CCM. In BCM, $D_3$ becomes zero at end of the switching period. So the value of $i_L$, $i_{LK}$ & $i_{LM}$ becomes zero. At the final end of this operation -the $i_{Lm}$ value is nearly equal to $I_L$-0.5$\Delta i_L$. If the $L_m$ is in CCM, its maximum value of current is to be semi of its ripple. It implies the $L_m$ is in CCM.

$$L_m \geq \frac{nD}{2f_s\left(\frac{M_{CCM}^2}{R_L} - \frac{D}{2Lf_s}\right)} \quad (33)$$

For operating the converter in CCM, the $L_{min}$ must be calculated. It operates in CCM when the normal value of inductor current is better than the semi of its ripple, using eqn (31) $L_{min}$ can be obtained as

$$I_L \geq \frac{\Delta i_L}{2} \Rightarrow L \geq -\frac{DR_L}{2M_{CCM}^2 f_S} \quad (34)$$

Figure 8 shows the current waveforms in BCM.

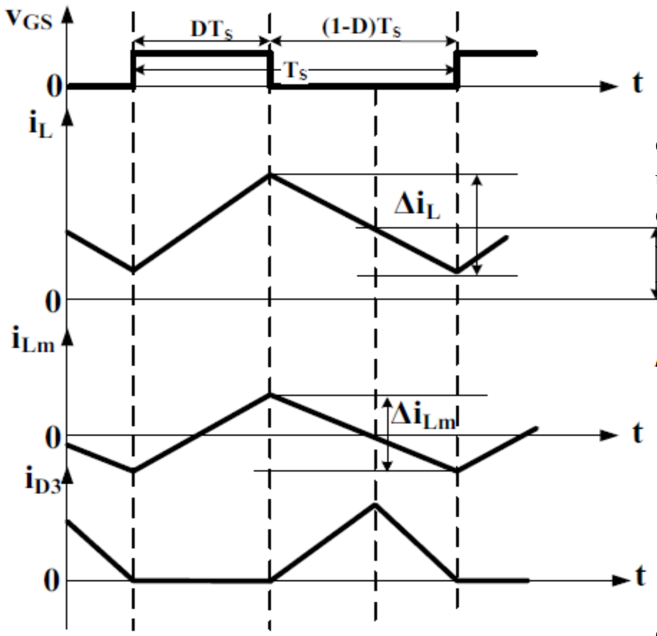


Figure 8. Current waveforms in BCM

## III. Design of the switching components

Voltage and current stress are obtained by selecting the appropriate semiconductors of the new converter, according to the working principle the stress voltages of diodes and switches are formulated as.

$$V_S = V_{D1} = V_{C1} = \frac{V_1}{1-D} \quad (35)$$

$$V_{D2} = V_{D3} = V_0 - V_{C2} = \frac{(n+1)V_1}{1-D} \quad (36)$$

The $D_{2(peak)}$ current is obtained from equation (19). The value of $S_{peak}$ and diode $D_{1(peak)}$ currents is as follows:

$$i_{s\ peak} = i_{D1\ peak} = \left(\frac{2n+2-nD}{D(1-D)}\right) I_0 + \left(\frac{1}{L} + \frac{n}{L_m}\right)\frac{DV_1}{2f_s} \quad (37)$$

Based on Fig. III and taking equation (37), the current value of $D_{3(peak)}$ can be written as given below:

$$\langle i_{D3}\rangle = I_0 = \frac{i_{D3\ peak}(2(1-D) - d_4)}{2} \Rightarrow i_{D3\ peak} = \frac{(n+2)I_0}{(n+1)(1-D)} \quad (38)$$

By neglect, the ESR of the $C_O$, the $V_O$ ripple of the new converter can be given as follow

$$V_{C0}(DT_S) = V_{C0}(0) + \frac{1}{C_0}\int_0^{DT_S} i_{c0}\ (t)dt \qquad |\Delta V_{C0}| = \frac{DV_0}{f_S R_L C_0} \quad (39)$$

According to [1], [18], [28], by taking into consideration a certain ripple value, $C_O$ size is designed using (39). Then, by taking the ESR of the selected capacitor, the voltage ripple is less than the desired voltage ripple. The peak-peak voltage across the ESR of the Capacitor $C_O$ can be taken as

$$\Delta V_{C_0}^{ESR} = r_{C_0}\ \Delta i_{C_0\ max} \Rightarrow \Delta V_{C_0}^{ESR} = r_{C_0}\left(\frac{(n+2)V_0}{R_L(n+1)(1-D)}\right) \quad (40)$$

## IV. Modelling of PI Controller

The enhanced PI controller is the commonly used control technique in electric vehicle applications. Figure 9 demonstrates the block diagram of the enhanced PI control technique

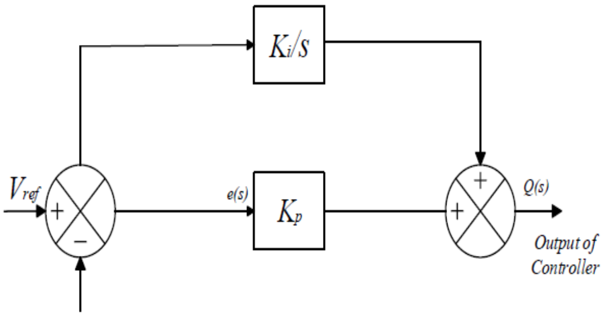


Figure 9. Block diagram of proposed PI controller for converter

The error signal $e(s)$ is sent to the PI controller i.e $K_p$ and output control signal Q(s) of the enhanced PI controller of the proposed system is:

$$Q(S) = \left[K_P + \left(\frac{K_i}{s}\right)\right] \times e(s)$$

## V. Modelling of FLC

The development of FLC is easier and provides effective flexibility for the sudden change in output loads. In addition, it provides effective and smarter dynamic responses and is very reliable in operation. The FLC set rules are defined below:

1. Gaussian Method.
2. Sigmoidal Method.
3. Trapezoidal Method.
4. Π Method.
5. Triangular Method.
6. Bell Method etc.

Figure 9a shows the Block diagram of the proposed FL controller for the converter.

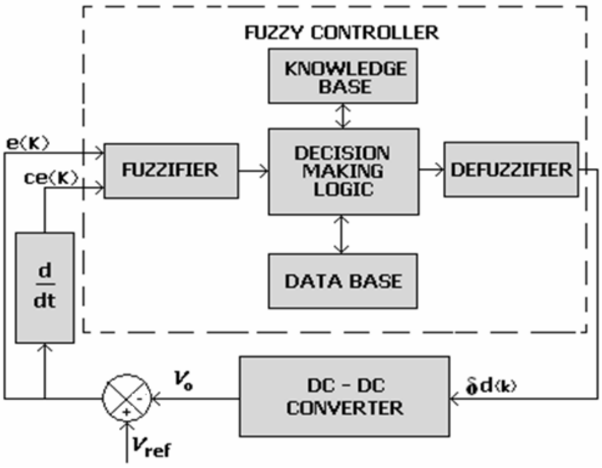


Figure 9a. Block diagram of proposed FL controller for converter

### 5.1 Fuzzification

The process of defining the fuzzification matches the input data with the predefined conditions with set rules to examine how well the condition of each rule matches that particular input instance. It gives a mathematical way to demonstrate each input and output variable in traditional language. Figures 9b, 9c, and 9d show the fuzzy membership function of the error input variable with 7 linguistics.

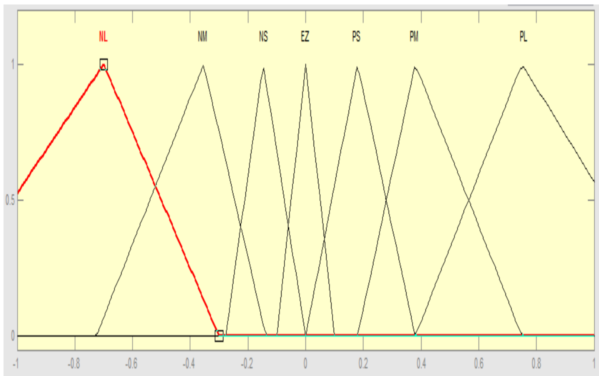


Figure 9b. Membership function for single input

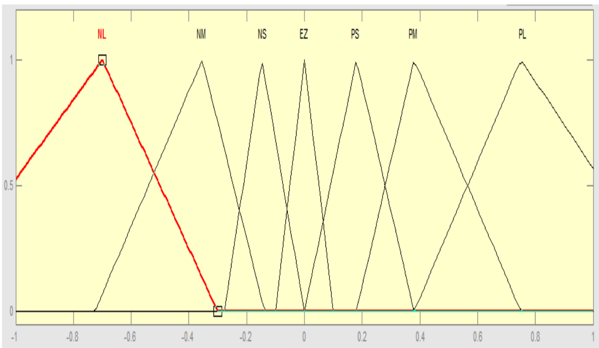


Figure 9c. Membership functions error for change in error

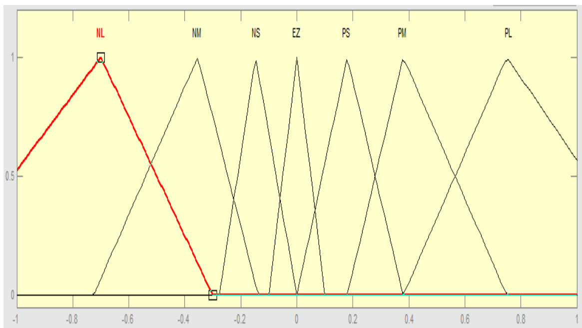


Figure 9d. Membership function for control signal

## VI. Simulation Results

The whole analysis is done in MATLAB/Simulink, and analysis takes part in three cases which gives an open loop of dc-dc converter in case I, PV fed dc-dc converter with PI and FL controllers in cases 2 and 3 respectively. Table 1 shows the specifications of the PV module and DC-DC converter.

Table 1. Circuit Parameters

| Specification | Parameters |
|---|---|
| PV Parameters | |
| $V_{OC}$ | 27V |
| $I_{SC}$ | 3.8A |
| Parasitic resistor (Ro) | 1Ω |
| Parasitic capacitor (Co) | 0.1mF |
| DC-DC Converter Parameters | |
| $V_{in}$ | 27V |
| $V_{out}$ | 290V |
| Capacitors | c1, c2, c3, c4=47MF |
| | c0 =180µF |
| Inductors | 320Mh |
| Coupled-Inductor | Lm=100µH |
| | n=2.1 |
| Switching frequency | 30Khz |

CASE (I): Open-loop simulation of new non-isolated coupled inductor-based high step-up DC-DC converter

Designed for 225 watts of power and 27 input voltages achieving a high dc voltage of nearly 300 volts having less duty cycle 0.6. The conventional boost converter can achieve the same output voltage, but it requires 0.94 duty cycle for 300 volts. Figure 10 shows the Simulink model of coupled inductor-based dc to dc converter

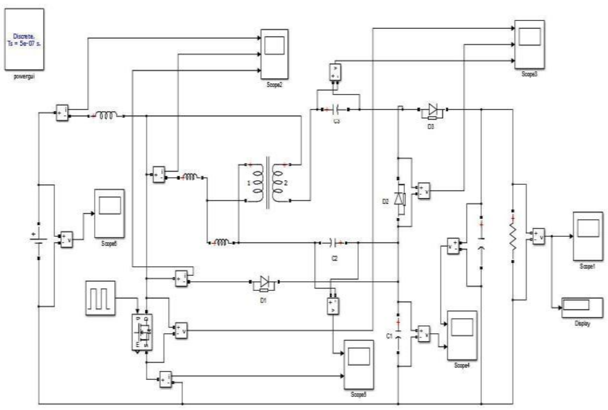

Figure 10. Simulink model of coupled inductor-based dc to dc converter

The output voltage response of the new converter is shown in Figure 10a. It's clear that the output voltage is 300V at 60% duty cycle operates 36% less than conventional converter.

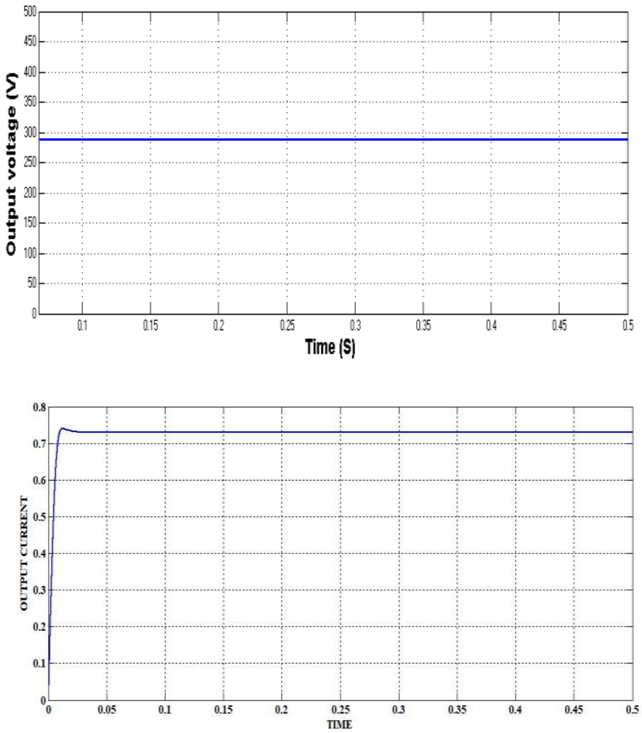


Figure 10a. Output voltage and output current response of coupled inductor-based DC-DC converter

Figure 10b shows the inductor and Diode current responses of coupled inductor converter.

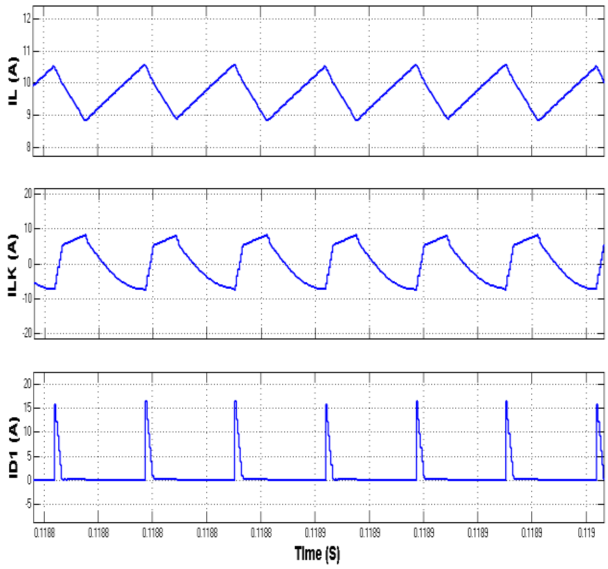


Figure 10b. Inductor and Diode current responses of coupled inductor converter

Figure 10c shows the capacitor voltage responses of coupled inductor converter.

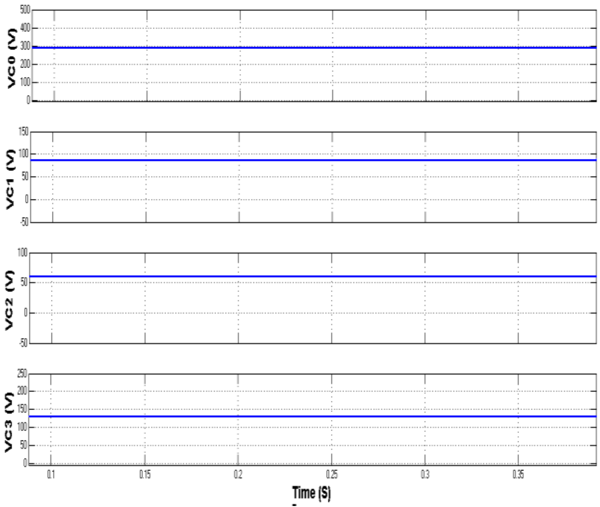


Figure 10c. Capacitor Voltage responses of coupled inductor converter

Figure 10d shows the Switch voltage responses (Diodes & main switch) of coupled inductor converter.

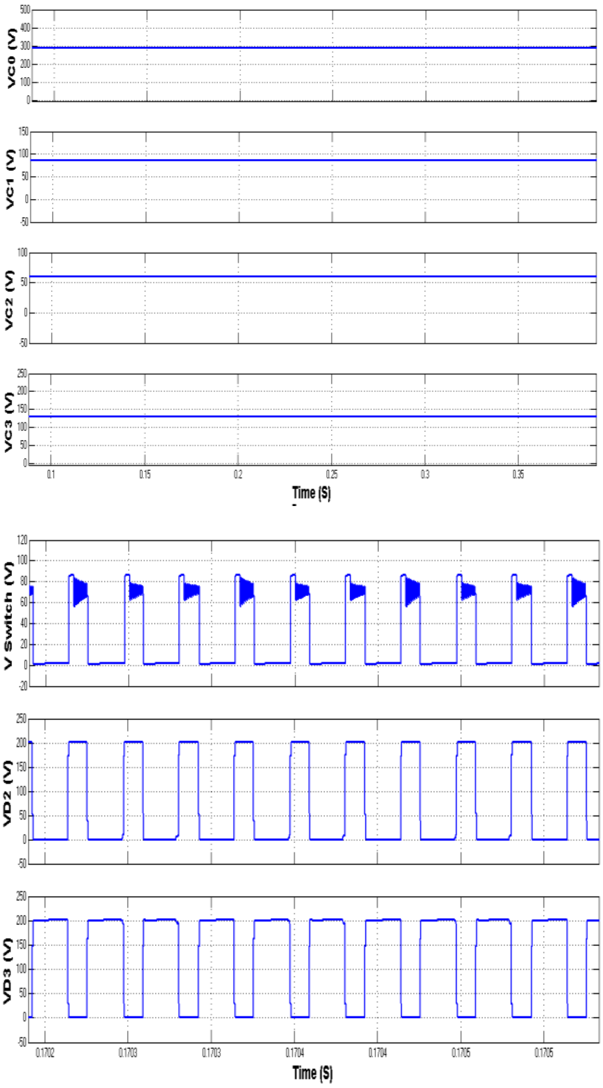


Figure 10d. Switch voltage responses (Diodes & main switch) of coupled inductor converter

Figure 6f shows the comparison of the voltage gains and switch stresses of the main switch for coupled inductor-based converter and boost converter. From the graphs, it is identified that the gain values of the coupled inductor-based converter are more than the boost converter for the same duty cycles. Also, the switch stresses are less for the coupled inductor-based converter compared to the boost converter. Thus, the coupled inductor-based converter is superior in operation to the boost converter and in further sections, the dynamic performance of this converter is verified for the load changes using the PI controller and Fuzzy logic controller.

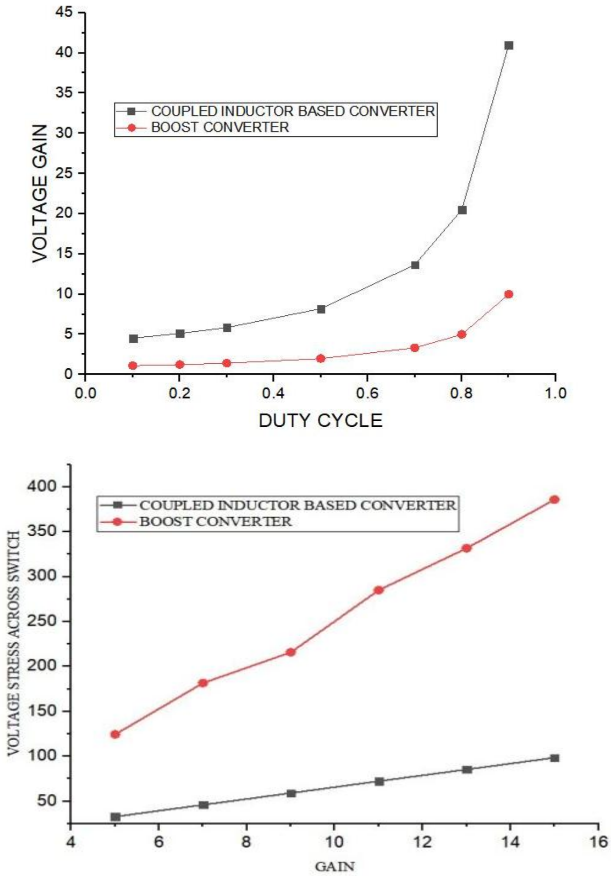


Figure 10e. Comparisons of voltage gains and switch stress of coupled inductor-based converter and boost converter

**CASE (II): closed-loop control simulation of PI-controlled coupled inductor based dc to dc converter**

Figure 11a gives the simulation diagram of the proposed converter at an input voltage is 27 V, load current varies from 0.35 to 0.72 A and Figure 11b shows the voltage and current responses of dc-dc converter using a PI controller.

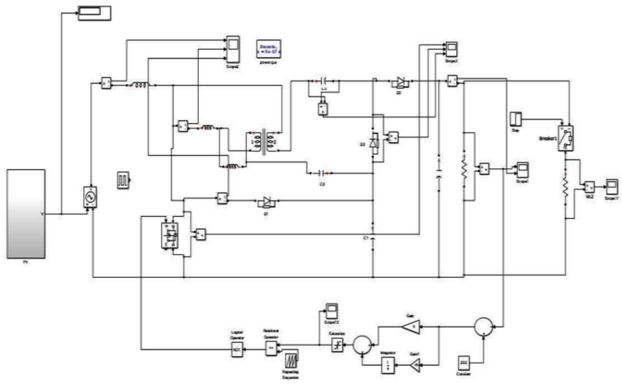

Figure
11a. Simulink model of PI-controlled coupled inductor based dc to dc converter

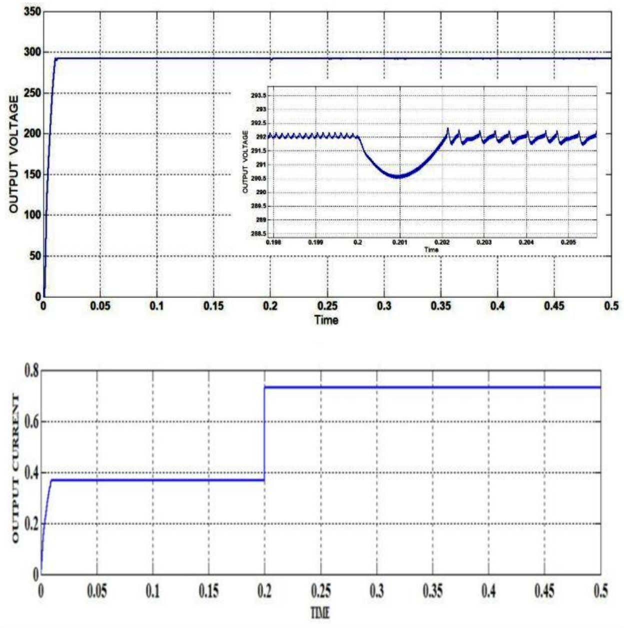


Figure 11b. Voltage and current responses of dc-dc converter using PI controller

**CASE (II): closed-loop control simulation of fuzzy controlled coupled inductor-based dc to dc converter**

The input voltage is 27 V, the output voltage 290V, and the load current are from 0.35 A to 0.72A with the FL controller.

Figure 12a gives the Simulink model of Fuzzy controlled coupled inductor based dc to dc Converter and Figure 12b shows the output voltage and current responses of FLC coupled inductor Converter for a sudden load change at 0.2 sec from 112.5W to 225W

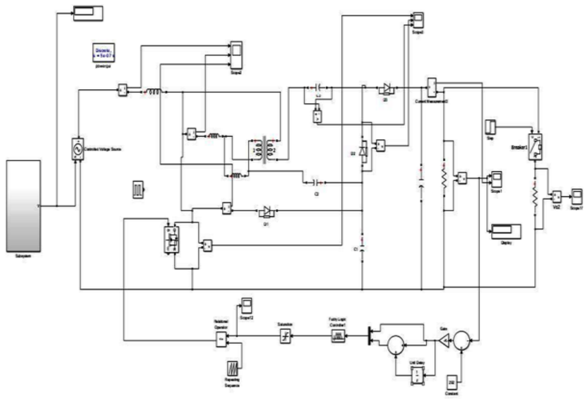

Figure 12a. Simulink model of Fuzzy controlled coupled inductor based dc to dc Converter

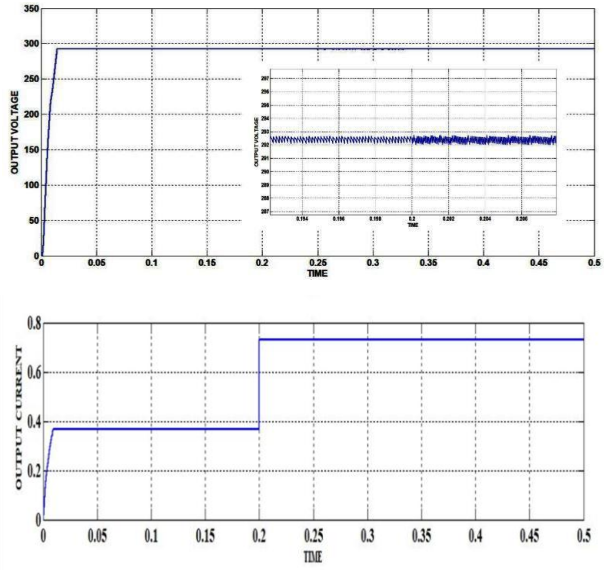


Figure 12b. Output voltage and current responses of FLC coupled inductor Converter for a sudden load change at 0.2 sec from 112.5W to 225W

## VII. Comparison Study

Comparison for both PI and FUZZY controlled coupled inductor based dc to dc Converter. Figure 13a presents the Output voltage responses of PI & Fuzzy controlled coupled inductor Converter for a sudden load change at 0.2 sec from 112.5W to 225W

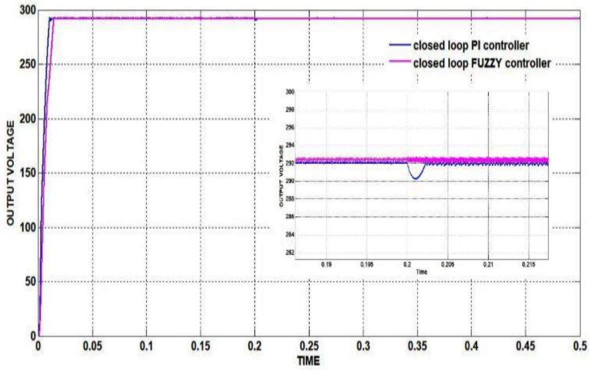


Figure 13a. Output voltage responses of PI & Fuzzy controlled coupled inductor Converter for a sudden load change at 0.2 sec from 112.5W to 225W

Figure 13b shows the Simulink model of the coupled inductor with fuzzy logic controller maintaining the stiff output voltage of 300V even under the changes in the input voltage from 27V to 15V.

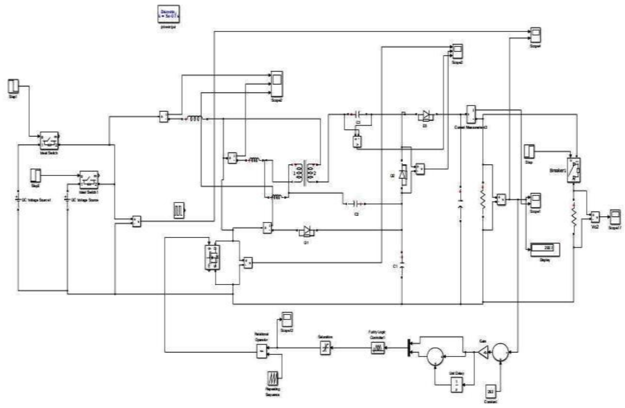

Figure 13b. Simulink diagram of a coupled inductor with voltage variations using a fuzzy logic controller

Figure 13c shows the output voltage response of 300V for the converter with fuzzy controller under the changes in the input voltage from 27V to 15V at 0.2 sec.

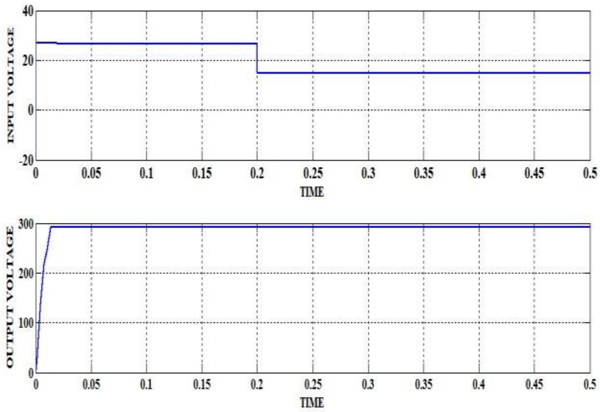


Figure 13c. Output voltage response for input voltage variations applied at 0.2 sec from 27V to 15V.

Figure 13d shows the comparison for both PI and fuzzy controller when sudden input voltage variations.

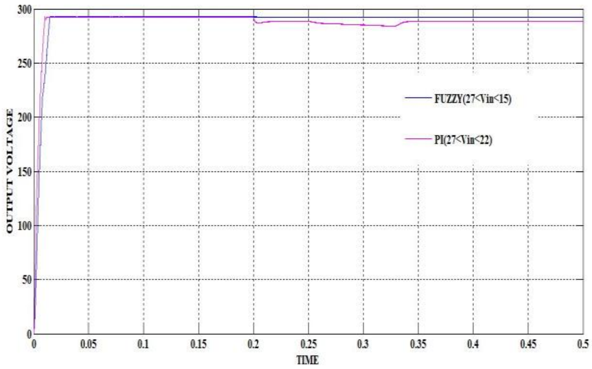


Figure 13d. Comparison for both PI and fuzzy controller when sudden input voltage variations

Thus, the fuzzy logic controller works effectively for the range of voltage variations at the input side from 15V to 27V and delivers a stiff voltage of 300V.

$$S = V_S I_S + \sum V_D I_D. \tag{41}$$

## VIII. Conclusion

A non-isolated DC-DC converter with high voltage gain is designed and simulated in MATLAB R2012b version. The same output voltage of 300V is achieved for a very smaller duty ratio of 0.65 when compared with the conventional boost converter. It comprises 3-diodes, 3-capacitors, 1-inductor, and a coupled inductor are utilized. The pressures switch S is reduced by utilizing the clamping circuit formed with diode $D_1$ and capacitor $C_1$. The dynamic response of the converter is analyzed for the disturbances on the load side from 112.5W to 225W at 0.2 sec and the output voltage is maintained constant by using the PI and FLC.  The PI-controlled converter settles to the desired voltage with a dip of 1.2V at the disturbance point (0.2sec), whereas the fuzzy logic-controlled converter gives a stiff voltage of 300V without any dip. Also, the fuzzy logic controller is verified for the disturbances at the input side for a range of 15V to the 27V input voltage.

## Declaration

- The authors declare that they have no known financial or non-financial competing interests in any material discussed in this paper.
- The authors declare that this article has not been published before and is not in the process of being published in any other journal.
- The authors confirmed that the paper was free of plagiarism.

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