POWER QUALITY IMPROVEMENT WITH CASCADED MULTILEVEL CONVERTER BASED STATCOM

MAHDI HEIDARI[1*], ABDONNABI KOVSARIAN[2] AND S. GHODRATOLLAH SEIFOSSADAT[2]

[1]Department of Electrical Engineering, University of Zabol, Zabol, Iran
[2]Department of Electrical Engineering, Shahid Chamran University of Ahvaz, Ahvaz, Iran.

[*]Corresponding author: m.heidari@uoz.ac.ir

(Received: 1st Oct 2017; Accepted: 22nd Feb 2018; Published on-line: 1st June 2018)

https://doi.org/10.31436/iiumej.v19i1.873

ABSTRACT: Static synchronous compensators (STATCOM) are increasingly implemented in power systems. Moreover, cascaded multilevel converters (CMC) are more frequently taken in consideration because of their strong capabilities. In this paper, the design and simulation of a multilevel STATCOM for voltage regulation of load is presented. Design of the passive components, active and reactive power controller, and balancer of capacitor voltage are parts of proposed system design. The pole placement method was used for the design of the controller. Simulation results with MATLAB/SIMULINK show good performance of voltage regulation in full load and dynamic load conditions.

ABSTRAK: Penyelaras pengimbang statik (STATCOM) semakin dilaksanakan dalam sistem kuasa. Selain itu, penukar pelbagai aras tingkatan (CMC) lebih diutamakan kerana mempunyai banyak kelebihan. Dalam kajian ini, reka bentuk dan simulasi bertingkat STATCOM bagi pelbagai voltan beban dibentangkan. Reka bentuk komponen pasif, penyelenggara kuasa aktif dan reaktif dan pengimbang voltan kapasitor adalah sebahagian daripada sistem yang dicadangkan. Bagi reka bentuk penyelenggara, kaedah penempatan titik telah digunakan. Hasil simulasi melalui MATLAB/SIMULINK menunjukkan keputusan yang baik pada regulasi voltan pada beban penuh dan pada keadaan beban dinamik.

KEYWORDS: *cascaded multilevel converter; STATCOM; power quality; voltage regulation; pole placement*

1. INTRODUCTION

In a deregulated power system, market and business are key factors in the design and operation of the network and lead to effective and efficient operation of the power system at all three levels: generation, transmission, and distribution. Therefore, power quality is of great importance, more so than any other issue, reactive dynamic power control is especially important in urban and local areas.

Flexible AC transmission systems (FACTS) are AC transmission systems combined with power electronics-based controllers that perform control of load flow and increase stability by controlling one or more system parameters such as voltage, phase angle, and impedance [1]. Among the FACTS controllers, parallel controllers, due to cost issues,

have shown their capabilities in a wide range of issues from transmission to distribution levels [2]. These controllers increase the power transmitted from transmission lines and improve the voltage profile along a line with an appropriate control of reactive power. In addition, parallel controllers can improve transient stability and cause the damping of power oscillations during an error [1]. Using high-speed power converters, parallel controllers can be used in distribution for applications such as voltage regulation [3], voltage balancing, reducing Flicker, and mitigating voltage sag [4].

Basically, all parallel controllers inject an additional current to the system at the point of common coupling (PCC). Parallel controller impedance that is connected to the PCC, creates a changing current. As long as the injected current has 90° phase difference with voltage, parallel controllers can only produce or absorb changing reactive power [2]. Parallel controllers include two groups: static reactive power (Var) compensators (SVC) and static synchronous compensators (STATCOM) [5]. SVC attracts or produces controllable reactive power by connecting the inductor or capacitor to or from the power system and therefore SVC is very slow for problems with rapid transition states. Using the semiconductor equipment with shutdown feature, power converters can be used at higher switching frequencies and provide faster response. This has caused voltage source converters (VSC) to be an important part of FACTS controllers, creating a parallel controller known as STATCOM, with its single-line diagram illustrated in Fig. 1 [1].

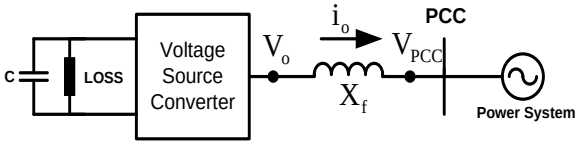

Fig. 1: single-line diagram of STATOM.

Among the structures of power converters that have been recently introduced, multilevel converters are useful structures that can be used in high power applications such as FACTS devices. Several structures of multilevel converters are presented, most notably Diode Clamed Multilevel Converter (DCMC) [6], Flying Capacitor Multilevel Converter (FCMC) [7], Generalized P2-cell Multilevel Converter (P2MC) [8], Cascaded Multilevel Converter (CMC) [7], Reversing Voltage Multilevel Converter (RVMLC) [9], and Modular Multilevel Converter (M2MC) [10]. With these converters, switches with lower nominal power can be used in medium voltage [2]. Among the diverse structures provided, the cascaded multilevel converter (CMC) has a possible and useful structure for reactive power compensation without voltage unbalancing [2, 11].

Cascaded multilevel converters are made with a number of identical H-bridge converters [12]. The modular structure not only simplifies the construction of the hardware, but also the overall system on power capability enables flexibility. Moreover, it has far fewer components compared to other structures and all its components are the same for any number of levels [5, 13]. A STATCOM structure based on CMC is shown in Fig. 2.

Several studies were performed on CMC-based STATCOM for improving dynamic response and stabilization of DC capacitor voltage [2, 5, 11]. According to the advantages of multilevel converters in power quality applications and CMCs in particular, this paper recaps the design and simulation of CMC-based multilevel STATCOM for load voltage regulation. Compared to the previous control strategies [14-17], the proposed method has

a higher performance for power quality improvement and is comparatively easy and has high practical value with easy hardware implementation. In the second section, investigation of factors affecting passive components of CMC-based multilevel STATCOM and its power circuit design to regulate the load voltage is done. The control algorithm, STATCOM control system design and modeling of the test system and multilevel STATCOM based on CMC are conducted in the third section and test system and CMC-based multilevel STATCOM in the fourth section with the MATLAB/SIMULINK software is simulated. Finally, conclusion is provided in the fifth section.

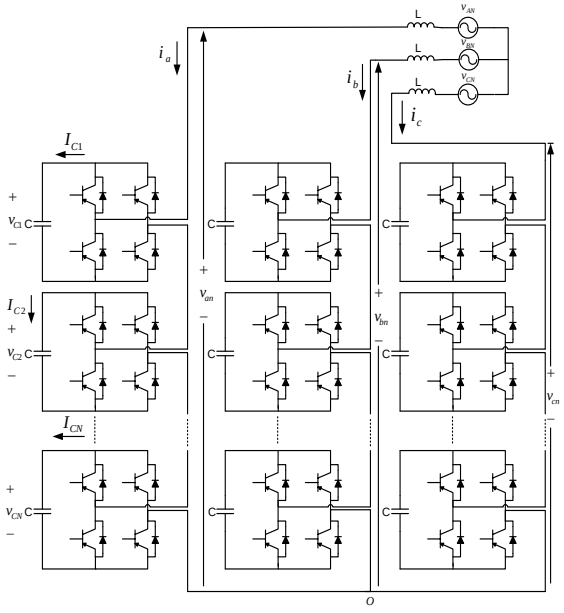

Fig. 2: CMC based STATCOM.

2. CMC-BASED MULTILEVEL STATCOM POWER CIRCUIT DESIGN FOR THE LOAD VOLTAGE REGULATION

2.1 Nominal Reactive Power Design of STATCOM

The test system is shown in Fig. 3 and its characteristics are given in Table 2 in the appendix. In this test system, constant and switchable loads are fed through a feeder and the purpose of applying STATCOM is to regulate the load voltage in nominal value.

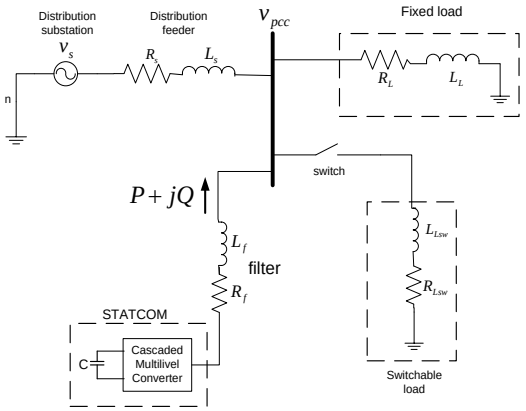

Fig. 3: Test system.

Assuming a full load condition and placement of STATCOM equivalent circuit in the test system shown in Fig. 4, the STATCOM nominal reactive power is designed for the load voltage regulation. By writing the KCL equation at PCC, we will have:

$$\frac{v_{pcc}-v_s}{R_s+jX_s}+\frac{v_{pcc}}{\frac{R_{loss}}{3}}+\frac{v_{pcc}}{R_{L_{tot}}+jX_{L_{tot}}}=-jI \tag{1}$$

By putting numerical values from Table 2, the voltage v_{pcc} can be obtained by:

$$v_{pcc}=(57.6574+0.5636I)+j(2.1144-0.6108I) \tag{2}$$

Since the purpose of applying STATCOM is to regulate the load voltage, voltage magnitude v_{pcc} must be equal to supply voltage and therefore nominal current and reactive power of the STATCOM is obtained by:

$$\left|v_{pcc}\right|=\sqrt{(57.6574+0.5636I)^2+(2.1144-0.6108I)^2}=64\Rightarrow I\approx 12A \tag{3}$$

$$Q_{STATCOM}=3\times 64\times 12=2304\,\text{var} \tag{4}$$

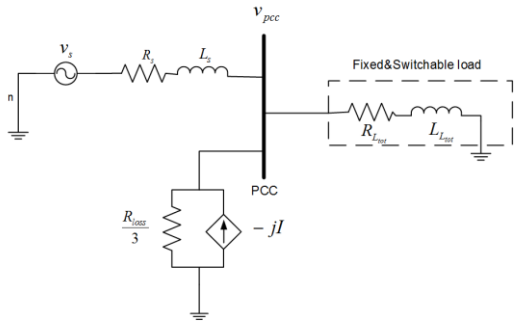

Fig. 4: Equivalent circuit of test system and STATCOM.

2.2 Design of Passive Components of STATCOM

The passive components in a STATCOM system are DC capacitors and a L_f reactor. Since passive components of a STATCOM system have a significant impact on system performance, design, and the factors affecting the DC capacitor, the reactor size will be detailed here.

2.2.1 DC Capacitor Design

Factors that affect the capacitance are voltage ripple [18], modulation index [19], harmonic distortion in output current and voltage of converter [20], and voltage overshoot [19]. The minimum value of DC capacitance is determined by overshoot and voltage ripple, while the maximum value is limited by cost.

Given the low rate of harmonics in the converter output voltage, DC capacitance is designed as follows [21]:

$$C_{dc}=\frac{Q}{\Delta V_{dc}} \tag{5}$$

where ΔV_{dc} is the maximum allowed voltage ripple of the capacitor voltage and Q is the charge of the capacitor. Maximum ripple voltage takes place in π/2 from each period. Thus, charge of the capacitor is in the form of Eq. (6):

$$Q = \int_0^{\frac{\pi}{2}} \sqrt{2}.I_{RMS}.\cos(2\pi ft)dt = \frac{I_{RMS}}{\sqrt{2}.\pi.f} \tag{6}$$

That I_{RMS} effective value of the converter current and f is frequency of system. By combining Eqn. (5) and (6), DC capacitance value is obtained.

$$C_{dc} = \frac{I_{RMS}}{\sqrt{2}.\pi.f.\Delta V_{dc}} \tag{7}$$

By inputting nominal values of the test system, multilevel STATCOM, and 10% allowed ripple of voltage, DC capacitance is obtained at 12 mF.

2.2.2 Factors Affecting the Size of Reactor

The reactor is the second passive component in STATCOM. The purpose of using the reactor is firstly the filtering of converter current harmonics, and secondly as reactive power coupler, i.e. the cause of reactive current. Factors that affect the size of the reactor are the converter output current harmonic distortion [22], performance range of the converter [23], and dynamic response of the system [24]. The minimum value of the reactor is determined by current harmonic distortion and the maximum value is determined by performance range of the converter and cost.

It is assumed for reactor design that the multilevel STATCOM output voltage and current is sinusoidal and the reactor resistance is ignored. Thus, inductance of the reactor is defined as follows [21]:

$$X_f = \frac{\frac{v_{o\max}}{\sqrt{2}} - v_{RMS}}{I_{RMS}} = \frac{\frac{N.V_{dc}}{\sqrt{2}} - v_{RMS}}{I_{RMS}} \tag{8}$$

where $v_{o\max}$ the maximum output voltage of the converter CMC, N is the number of H-bridge converters in each phase, v_{RMS} is the effective phase voltage of the system, and I_{RMS} is the effective current of system. By inputting nominal values of the test system and multilevel STATCOM, the inductance of the reactor is obtained as $L_f = 2.2mH$. Because the reactor resistance is neglected, reactor resistance is 0.1 of the reactor reactance and is placed equal to $R_f = 0.1X_f = 0.1\Omega$.

3. CONTROL ALGORITHM AND CMC BASED STATCOM CONTROL SYSTEM DESIGN

3.1 Active and Reactive Power Control Algorithm

According to the theory of instantaneous reactive power that was presented by Akagi et al. in 1983 [25, 26], active and reactive power exchanged between power and STATCOM systems are defined as follows:

$$P = v_{pccd}i_d + v_{pccq}i_q \tag{9}$$

$$Q = -v_{pccq} i_d + v_{pccd} i_q \tag{10}$$

If we put $v_{pccq} = 0$ in the above equations, the equations are as follows:

$$P = v_{pccd} i_d \tag{11}$$

$$Q = v_{pccd} i_q \tag{12}$$

As can be seen in these equations, active and reactive power is controlled by i_d and i_q respectively. In fact, active and reactive power control is carried out completely independently. If the STATCOM produces reactive power, then i_q will be negative and if STATCOM attracts reactive power, i_q will be positive. Similarly, if the STATCOM produces active power, then i_d will be positive and if STATCOM attracts active power, i_d will be negative [27].

3.2 CMC Based STATCOM Control System Design

Figure 5 shows the multilevel STATCOM controller. In this controller, first, voltages of v_{pcca}, v_{pccb} and v_{pccc}, and currents of i_a, i_b and i_c can be changed to v_{pccd}, v_{pccq}, i_d and i_q using Park's transformation matrix. Angle θ in Park's transformation matrix is obtained by phase-locked loop (PLL). Figure 6 shows a block diagram of PLL [28]. According to the block diagram and description of previous section, v_{pccq} is first compared by zero value and the difference between these two is given to PI controller. Since reference coordination is synchronous, the PI controller output is summed with $\omega = 120\pi$. By integrating the obtained value, angle θ is obtained.

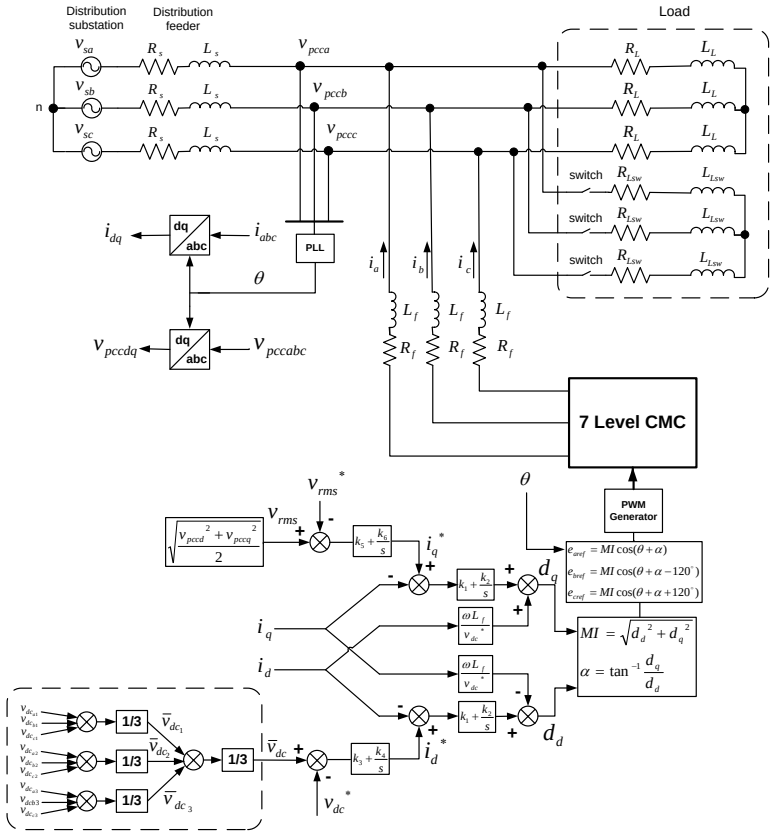

Fig. 5: Multilevel STATCOM controller.

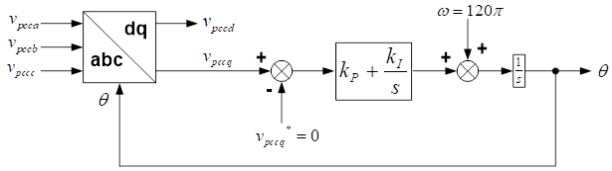

Fig. 6: Block diagram of PLL [28].

Since the purpose of applying multilevel STATCOM is voltage regulation, the effective voltage in PCC is compared with the desired value in the loop Q and is given to the PI controller. PI controller output is the reactive current value that multilevel STATCOM should produce or attract. In other words, the current is the reference value of i_q. Then, i_q is compared with the reference value of itself and is given to the PI controller. The controller output forms switching function of Q axis.

In loop D, the average capacitor voltage is initially compared with the reference value and is given to the PI controller. The PI controller output is the active current value that multilevel STATCOM should produce or attract. In other words, the current is reference value of i_d. Then, i_d is compared with the reference value of itself and is given to the PI controller. The controller output forms switching function of D axis. When switching functions of axes D and Q were obtained, their amplitude and angle are estimated. These values are initial amplitude and phase of reference signals of PSPWM.

To determine the coefficients k_1, k_2, k_3, k_4, k_5 and k_6 of PI controllers, the closed loop equations are obtained based on the test system, multilevel STATCOM, and controller. Equations (13) and (14) are the average model of CMC based STATCOM [5] and open loop state equations of the studied system and multilevel STATCOM in ABC coordination.

$$\begin{cases} \dfrac{d\vec{i}_{abc}}{dt} = \dfrac{1}{L_f} v_{dc}.\vec{D}_{abc} - \dfrac{1}{L_f}\vec{v}_{pccabc} - \dfrac{R_f}{L_f}\vec{i}_{abc} \\ \dfrac{dv_{dc}}{dt} = -\dfrac{1}{R_{lossj}.C} v_{dc} - \dfrac{1}{3.C}.\vec{d}_{abcj}{}^{T}.\vec{i}_{abc} \quad , j = 1,...,N \end{cases} \tag{13}$$

$$\begin{cases} \dfrac{d\vec{i}_{sabc}}{dt} = \dfrac{1}{L_s}\vec{v}_{sabc} - \dfrac{1}{L_s}\vec{v}_{pccabc} - \dfrac{R_s}{L_s}\vec{i}_{sabc} \\ \dfrac{d\vec{i}_{Labc}}{dt} = \dfrac{1}{L_{L_{tot}}}\vec{v}_{pccabc} - \dfrac{R_{L_{tot}}}{L_{L_{tot}}}\vec{i}_{Labc} \quad , \vec{i}_{Labc} = \vec{i}_{sabc} + \vec{i}_{abc} \\ \dfrac{d\vec{i}_{abc}}{dt} = \dfrac{N}{L_f} v_{dc}.\vec{d}_{abc} - \dfrac{1}{L_f}\vec{v}_{pccabc} - \dfrac{R_f}{L_f}.\vec{i}_{abc} \\ \dfrac{dv_{dc}}{dt} = -\dfrac{1}{R_{loss}.C} v_{dc} - \dfrac{1}{3.C}\vec{d}_{abc}{}^{T}.\vec{i}_{abc} \end{cases} \tag{14}$$

In these equations: $\vec{i}_{abc}=\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \vec{D}_{abc}=\begin{bmatrix} D_a \\ D_b \\ D_c \end{bmatrix}, \vec{d}_{abcj}=\begin{bmatrix} d_{aj} \\ d_{bj} \\ d_{cj} \end{bmatrix}$ and $\vec{v}_{pccabc}=\begin{bmatrix} v_{pcca} \\ v_{pccb} \\ v_{pccc} \end{bmatrix}$. Also, $R_{L_{tot}}$ and $L_{L_{tot}}$ are load resistance and inductance respectively in full load condition (constant and switchable load on the circuit). By multiplying the Eqn. (14) in park transformation matrix, open-loop model in DQO coordination is obtained as Eqn. (15). Since the test system was a three-phase three-wire, the axis O is ignored.

$$\begin{cases} \dfrac{d\vec{i}_{sdq}}{dt}=\dfrac{1}{L_s}\vec{v}_{sdq}-\dfrac{1}{L_s}\vec{v}_{pccdq}-\begin{bmatrix} \dfrac{R_s}{L_s} & -\omega \\ \omega & \dfrac{R_s}{L_s} \end{bmatrix}\vec{i}_{sdq} \\ \dfrac{d\vec{i}_{Ldq}}{dt}=\dfrac{1}{L_{L_{tot}}}\vec{v}_{pccdq}-\begin{bmatrix} \dfrac{R_{L_{tot}}}{L_{L_{tot}}} & -\omega \\ \omega & \dfrac{R_{L_{tot}}}{L_{L_{tot}}} \end{bmatrix}\vec{i}_{Ldq} \quad ,\vec{i}_{Ldq}=\vec{i}_{sdq}+\vec{i}_{dq} \\ \dfrac{d\vec{i}_{dq}}{dt}=\dfrac{N}{L_f}v_{dc}.\vec{d}_{dq}-\dfrac{1}{L_f}\vec{v}_{pccdq}-\begin{bmatrix} \dfrac{R_f}{L_f} & -\omega \\ \omega & \dfrac{R_f}{L_f} \end{bmatrix}\vec{i}_{dq} \\ \dfrac{dv_{dc}}{dt}=-\dfrac{1}{R_{loss}.C}v_{dc}-\dfrac{1}{2.C}\vec{d}_{dq}{}^{T}.\vec{i}_{dq} \end{cases} \tag{15}$$

In these equations i_{sd} , i_{sq} , i_d , i_q and v_{dc} are state variables, d_d and d_q are control variables, v_{sd} and v_{sq} are input variables, respectively. The state variables in these equations are $x=\begin{bmatrix} i_{sd} & i_{sq} & i_d & i_q & v_{dc} & i_d^* & i_q^* & d_d & d_q \end{bmatrix}$. By linearization of equations at the operating point and applying a pole placement method for designing PI controllers, the gains of PI controllers are obtained to achieve optimal response and damping as $k_1=0.1$, $k_2=100$, $k_3=1$, $k_4=30$, $k_5=0.5$ and $k_6=100$ to achieve optimal response and damping. Table 1 shows eigenvalues of the test system and multilevel STATCOM with or without controller.

Table 1: Eigenvalues of system in full load condition.

Eigenvalues of system and Multilevel STATCOM	**Eigenvalues of system, multilevel STATCOM and controller**
$-242.37\pm384.34j$	$-1666\pm807j$
$-159.91\pm404.5j$	$-862.04\pm842.17j$
-31.43	$-221.35\pm378.38j$
	-33.78
	$-14.44\pm23.68j$

Because of different carrier signals, unbalancing usually occurs in capacitor voltage. In practice, this unbalance increases due to the lack of uniformity in components. Therefore, we need a balanced capacitor voltage.

Figure 7 shows the block diagram of the voltage capacitor balancer [29]. Each of the capacitor voltages is compared with its nominal value and is given to the PI controller. The controller output changes the angle that is deduced from the angle of reference signal related to its H-bridge converter.

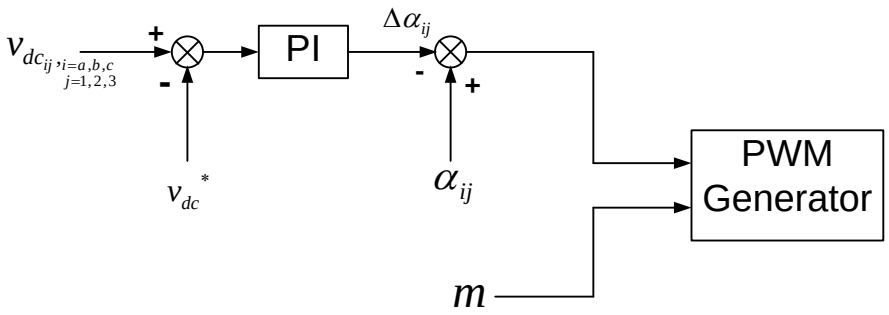

Fig. 7: Block diagram of capacitor voltage balancer [29].

4. SIMULATION

In this section, simulation of the system is presented using the MATLAB/SIMULINK software.

4.1 Simulation in Full Load Condition

In a full load condition, both constant and switchable loads are in circuit. A 7 level CMC converter with PSPWM control method was implemented. Figure 8 shows PSPWM switching control for a 7 level CMC converter. Figure 9 shows the output voltages of the CMC converter. Figures 10 and 11 respectively show the load voltages and effective phase voltages in the PCC. As can be seen, effective voltage of the load is regulated with good speed and accuracy at the nominal value of 45.5 volts, which reflects the good performance of the controller.

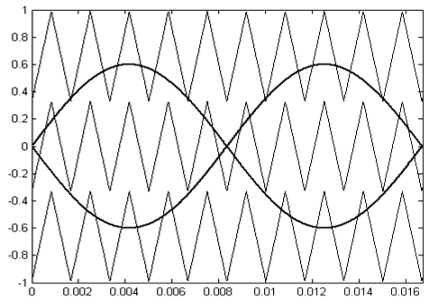

Fig. 8: PSPWM switching control for the 7 level CMC converter.

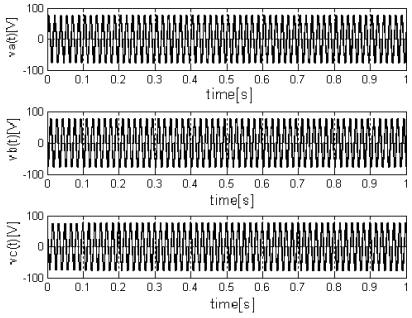

Fig. 9: Output voltages of the CMC converter.

Figures 12 and 13 respectively show the output current of a multilevel STATCOM and current of the Q axis(i_q). As can be seen, multilevel STATCOM is capable of injecting reactive current in less than 200 msec. Figure 14 shows the FFT analysis of

output current of multilevel STATCOM. As can be seen from the figure, the total harmonic distortion of the output current is 3.82%, which is less than 5% to meet the IEEE 519 standard. The average voltage of the capacitors is shown in Fig. 15. The average voltage of the capacitors is fixed completely at the nominal value of 25 volts.

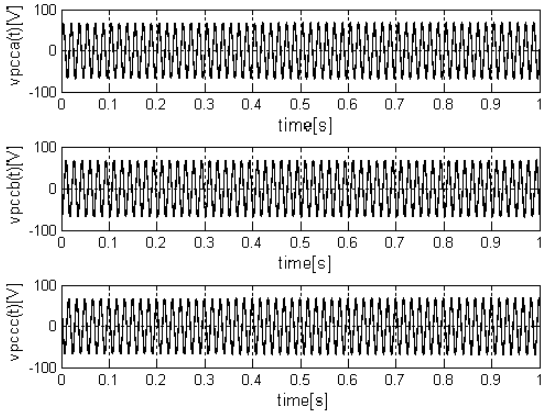

Fig. 10: Load voltages.

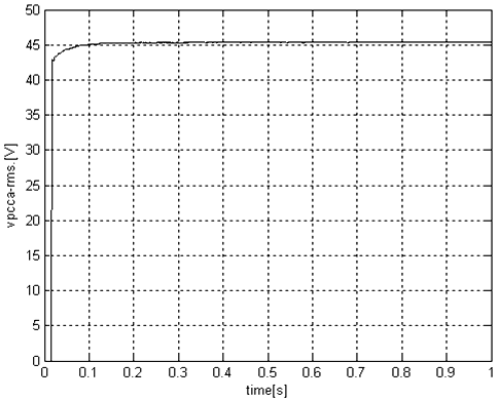

Fig. 11: Effective phase voltage in the PCC.

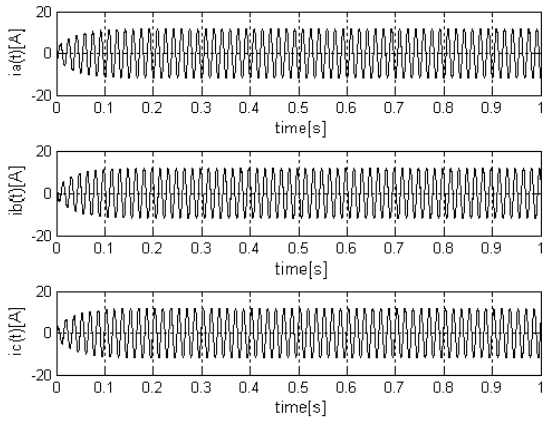

Fig. 12: Output current of the multilevel STATCOM.

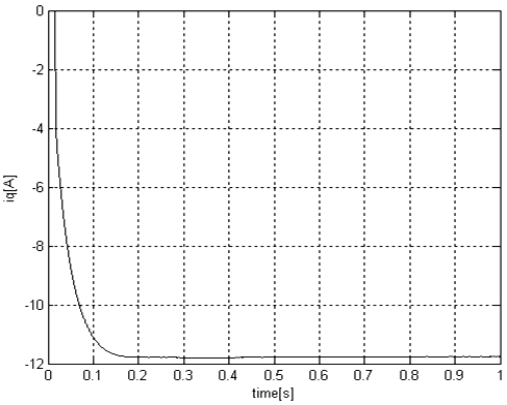

Fig. 13: Current of the Q axis (i_q).

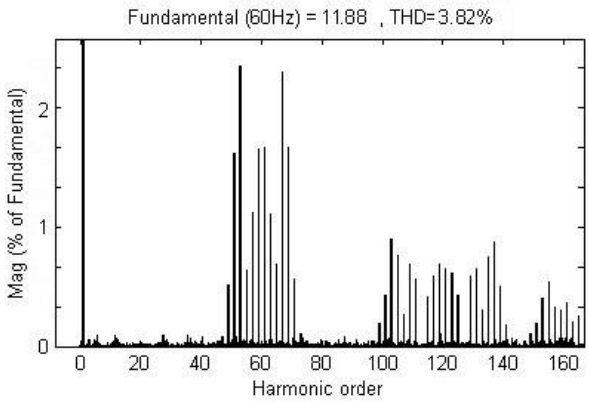

Fig. 14: FFT analysis of output current of the multilevel STATCOM.

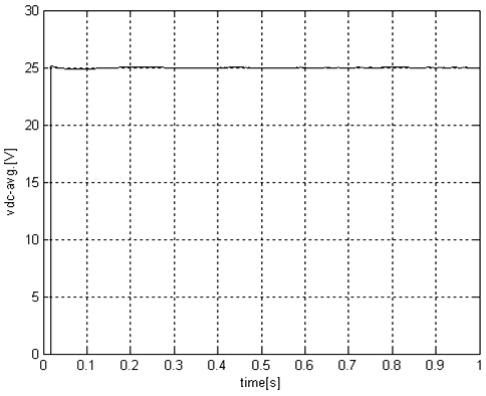

Fig. 15: Average voltage of the capacitors.

4.2 Simulation in Dynamic Conditions

In this case, a constant load is in the circuit. At the time of 500 msec, a switchable load enters the circuit and finally, the switchable load is output from the circuit at the time of 1 second. Figures. 16 and 17 show effective phase voltage in the PCC and current of the Q axis (i_q) respectively. As can be seen, effective voltage of load is regulated with good speed and accuracy at the nominal value of 45.5 volts, which reflects the good performance of the controller in dynamic conditions.

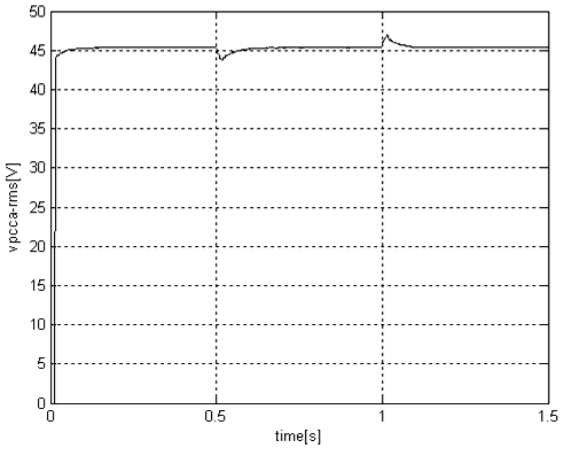

Fig. 16: Effective phase voltage in the PCC.

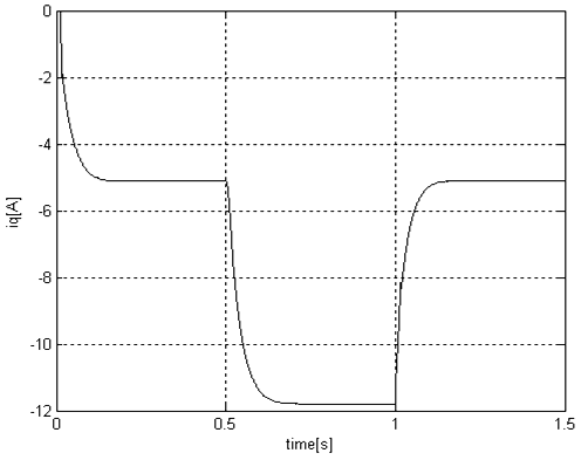

Fig. 17: Current of the Q axis (i_q).

5. CONCLUSION REMARKS

In this paper, the design and simulation of a multilevel STATCOM to regulate load voltage are provided. Among conventional multilevel converters, the cascade multilevel converter was chosen for use in the STATCOM due to fewer components and the simplicity of control. For the cascade multilevel converter output voltage control, the phase-shifted sinusoidal pulse width modulation method (PSPWM) was selected due to a better harmonic spectrum and simplicity of producing the switching angles.

A cascaded multilevel converter STATCOM design was presented in two parts. In the first part, the multilevel STATCOM to regulate load voltage in the test system was designed and its nominal reactive power was obtained. Also, design of multilevel the STATCOM passive components, based on cascade multilevel converter, was presented in this section. Due to the factors that affect the size of these components, design of these components was conducted optimally. In the second part, the multilevel STATCOM control system was designed. The design by pole placement method to achieve the optimal dynamic properties was performed. To balance the voltage of the capacitors, a voltage balancer was added to the control system. The simulation results showed dynamic and steady state responses of the control system at full load and dynamic conditions with good speed and accuracy in the nominal value by balancing and stabilizing the voltage of capacitors. The proposed method has a higher performance for power quality improvement and is comparatively easy and possesses a high practical value with easy hardware implementation.

REFERENCES

[1] Hingorani NG, Gyugyi L. (2000) Understanding facts, IEEE press.

[2] Sirisukprasert S, Huang AQ, Lai J.-S. (2003) Modeling, analysis and control of cascaded-multilevel converter-based STATCOM. Power Engineering Society General Meeting, 2561-2568.

[3] Xu Y, Li F. (2014) Adaptive PI control of STATCOM for voltage regulation. IEEE Transactions on Power Delivery, 29(3):1002-1011.

[4] Elnady A, Salama MM. (2005) Unified approach for mitigating voltage sag and voltage flicker using the DSTATCOM. IEEE Transactions on Power Delivery, 20(2):992-1000.

[5] Sirisukprasert S. (2004) The modeling and control of a cascaded-multilevel converter-based STATCOM. Virginia Tech.

[6] Rodriguez J, Lai J-S., Peng FZ. (2002) Multilevel inverters: a survey of topologies, controls, and applications. IEEE Transactions on Industrial Electronics, 49(4):724-738.

[7] Lai J-S, Peng FZ. (1996) Multilevel converters-a new breed of power converters. IEEE Transactions on Industry Applications, 32(3):509-517.

[8] Peng F. Z. (2001) A generalized multilevel inverter topology with self voltage balancing. IEEE Transactions on industry applications, 37(2): 611-618.

[9] Najafi E, Yatim A, Samosir A. (2008) A new topology-Reversing Voltage (RV) for multilevel inverters. in Power and Energy Conference, 604-608.

[10] Siemaszko D, Antonopoulos A, Ilves K, Vasiladiotis M, Ängquist L, Nee H-P. (2010) Evaluation of control and modulation methods for modular multilevel converters. in Power Electronics Conference (IPEC), 746-753.

[11] Liang Y, Nwankpa C. (1999) A new type of STATCOM based on cascading voltage-source inverters with phase-shifted unipolar SPWM. IEEE Transactions on Industry Applications, 35(5):1118-1123.

[12] Rashid MH. (2009) Power electronics: circuits, devices, and applications. Pearson Education India.

[13] Khomfoi S, Tolbert LM. (2007) Multilevel power converters. Power electronics handbook, 451-482.

[14] Tavana MR, Khooban MH, Niknam T. (2017) Adaptive PI controller to voltage regulation in power systems: STATCOM as a case study. ISA Transactions, 66:325-334.

[15] Park J, Yu J, Kim J, Kim M, Kim K, Han S. (2016) Frequency/Voltage Regulation with STATCOM with Battery in High Voltage Transmission System. IFAC-PapersOnLine, 49(27):296-300.

[16] Wang K, Crow ML. (2011) Power system voltage regulation via STATCOM internal nonlinear control. IEEE Transactions on Power System, 26(3):1252-1262.

[17] Augustine A, Paul E, Prakash RD, Balakrishna BM, Xavier R. (2016) Voltage regulation of STATCOM using fuzzy self tuning PI controller. International Conference on Circuit, Power and Computing Technologies (ICCPCT).

[18] Hannan MA. (2012) Effect of DC Capacitor Size on D-STATCOM Voltage Regulation Performance Evaluation. Przegląd Elektrotechniczny, 88(12a):243-246.

[19] Min Z, Yiwei Z, Libing C. (2014) DC Capacitor Voltage Control Strategy for the Cascaded STATCOM. Open Automation and Control Systems Journal, 6:1415-1425.

[20] Pulikanti SR, Konstantinou G, Agelidis VG. (2012) DC-link voltage ripple compensation for multilevel active-neutral-point-clamped converters operated with SHE-PWM. IEEE Transactions on Power Delivery, 27(4):2176-2184.

[21] Hawley JC. (2004) The modeling and simulation of a cascaded three-level converter-based SSSC. Virginia Polytechnic Institute and State University.

[22] Cetin A. (2007) Design and implementation of a voltage source converter based STATCOM for reactive power compensation and harmonic filtering. MIDDLE EAST TECHNICAL UNIVERSITY.

[23] Gultekin B, Ermis M. (2013) Cascaded multilevel converter-based transmission STATCOM: System design methodology and development of a 12 kV±12 MVAr power stage. IEEE transactions on power electronics, 28(11):4930-4950.
[24] Zhang JL. (2011) The design of STATCOM control system. in Applied Mechanics and Materials, 1631-1635.
[25] Akagi H, Kanazawa Y, Fujita K, Nabae A. (1983) Generalized theory of instantaneous reactive power and its application. Electrical engineering in Japan, 103(7):58-66.
[26] Heidari M. (2015) Improving the Power Quality of Wind Power Plants through Modifying the Instantaneous Active and Reactive Power Theory. International Journal of Renewable Energy Research, 5(3):722-731.
[27] Heidari M, Kovsarian A, Seifossadat S. (2011) Detailed Analysis of Cascaded Multilevel Converter Based STATCOM. International Review on Modelling and Simulations, 4(2):507-516.
[28] Yang Z. (2007) Digital Controller Design for Cascaded-Multilevel-Converter Based STATCOM Systems.
[29] Peng FZ, Lai J-S, McKeever JW, VanCoevering J. (1996) A multilevel voltage-source inverter with separate DC sources for static var generation. IEEE Transactions on Industry Applications, 32(5):1130-1138.