i-ETC: ISEL Academic Journal of Electronics, Telecommunications and Computers
CETC2011 Issue, Vol. 2, n. 1 (2013) ID-17

Design Methologies for Integrated Inductor-Based Soft-Switching DC-DC Converters

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Keywords: High switching frequency, Quasi-Resonant topologies, CMOS integrated circuits, Power management.

Abstract: This paper presents a study on resonant converter topologies targeted for CMOS integration. Design methodologies to optimize efficiency for the integration of Quasi-Resonant and Quasi-Square-Wave converters are proposed. A power loss model is used to optimize the design parameters of the power stage, including the driver circuits, and also to conclude about CMOS technology limitations. Based on this discussion, and taking as reference a 0.35µm CMOS process, two converters are designed to validate the proposal: a Quasi Resonant boost converter operating at 100MHz and a Quasi-Square-Wave buck converter operating at 70MHz. Simulation results confirm the feasibility of these topologies for monolithic integration.

1 INTRODUCTION

Power management circuits for battery powered portable electronic equipment are being more demand, imposing the research on very efficient solutions. In some of these equipments the difference between the battery and the circuit voltage are significant. For this kind of applications the use of inductor-based switching topologies in the conception of integrated DC-DC converters in CMOS technology have inherent advantages, in order to achieve good performances and compactness, at low cost.
The main design specifications for an inductor-based CMOS DC-DC converter are usually the ratio between the input and output voltages, the output power or load current, and the output voltage ripple. Nevertheless, additional variables such as the switching frequency and the inductor current ripple have also to be considered, since they have a direct impact on Silicon footprint, efficiency and system Electromagnetic Interference (EMI).
The fully integration of an inductor-based DC-DC converter in CMOS technology brings new challenges. The inductor and capacitance integration are restricted to low values, when compared with the discrete implementation, due to the available Silicon area. The low value integrated capacitors present reasonable behaviour and are normally used on mixed-signal. However, integrated inductors on standard CMOS process are only available for a few nH and specifically target for RF-CMOS applications.
Many authors have presented solutions with the objective of fully integrate switch-mode DC-DC buck converters [1-11]. Distinct solutions have been proposed. Some of the solutions are based on Discontinuous Conduction Mode (DCM) operation, in order to reduce the filter inductor to an acceptable value for CMOS, below 20 nH [7,9]. However, DCM operation implies overstress on power transistors for the same output load current. Other solutions make use of the stacked chip concept to perform a System in a Package (SiP) [8], which are not cost effective [1, 9].
Finally another approach is supported on the research of new design methodologies that leads to full integration, maintaining specifications competitive when compared with other hybrid and costly solutions [1-6].
It is well known that the physical dimensions and consequently the parasitic impedances of the filter passive components are greatly reduced as the converter switching frequency increases. In that case, the increase in the switching frequency could become the key parameter for full integration. For very high switching frequency the power transistors

and respective driver power losses dominate the losses on the converter [2], mainly due to the increase of the switching losses, turning the design of the power stage even more relevant [1-6, 12]. Although, the study of optimization methods on the design of the converters power stage [1-6, 12], all the solutions presented are based on hard-switching. So, the study of alternative solutions that could present lower switching losses maintaining high efficiency at high switching frequency is a major challenge. Among the Power Electronics DC-DC converters circuit topologies, the soft-switching topologies [13, 14, 15] are distinguished by their efficiency and low Electromagnetic Interference (EMI). Thus, the use of soft switching techniques appears attractive to minimize noise and switching losses [16].

The objective of this paper is to present design methods based on the analytical loss model of the power stage described on [12] for soft-switching topologies.

On section 2 the ZVS (zero voltage switch) Quasi Resonant converters are introduced discussing the necessity of defining a design procedure tailored for CMOS integration. A design procedure based on the theoretical operation for a boost converter is presented, which contemplates the power transistors and respective driver circuit optimization. Section 3 introduces the ZVS Quasi Square Wave converters. A design method for the buck topology with power transistors and respective driver circuit optimization is also presented. Several simulation results based on a standard 0.35 μm CMOS process are shown in section 4 for the two types of resonant switching converters, in order to verify and validate the viability of the theoretical approach. Conclusions are presented in section 5.

2 QUASI-RESONANT CONVERTERS

Quasi-Resonant Converters are obtained from conventional PWM (Pulse Width Modulation) converters by using resonant switches. The difference between these switches and the conventional PWM switches is the inclusion of an inductor and a capacitor, as shown in Figure 1, in order to allow ZCS (zero current switch) (a), or ZVS (zero voltage switch) (b).

As a consequence, theoretically, switching frequency can be increased with reduced switching losses and increased power density for integration purposes.

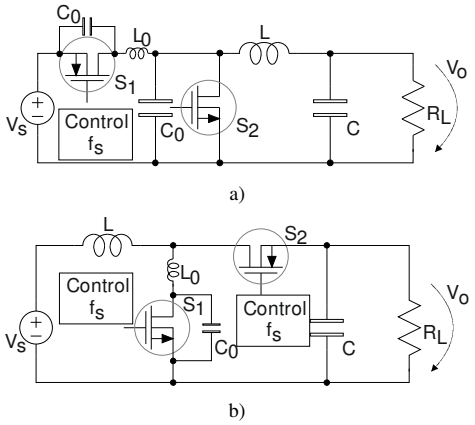

Fig. 1. a) Buck ZCS QR converter; b) Boost ZVS QR converter.

For monolithic integration in CMOS technology, the use of intrinsic MOSFET transistor capacitance as the resonant capacitor is a possibility. However, this is only valid for ZVS topologies. In fact, MOSFET parasitic capacitances distribution in ZCS converters, do not match with the specific resonant capacitor C_0, as can be confirmed in Figure 1 a). Furthermore, maximum current on the active switch is, at least, the double of the maximum current on a PWM equivalent converter [17]. These aspects reinforce the use of ZVS topologies for CMOS integration. For these reasons only the ZVS topologies are considered in this work.

2.1 Boost Quasi-Resonant Converter Theoretical Operation

A detailed steady state analysis of the ZVS-QR buck topology is presented in [18]. Based on that analysis, a design procedure for discrete ZVS-QR buck converter is developed in [15]. This study can be extended for the boost topology only with some modifications.

The resonant circuit, composed by L_0 and C_0, dominates the operation and mainly define the converter characteristics. For better comprehension consider the following parameters of the converter: characteristic impedance Z_0, the resonant frequency f_0, the normalized load resistance Q and the conversion ratio M:

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \quad (1.a) \qquad f_0 = \frac{1}{2 \cdot \pi \cdot \sqrt{L_0 \cdot C_0}} \quad (1.b)$$

$$Q = \frac{R_L}{Z_0} \quad (1.c) \qquad M = \frac{V_O}{V_I} \quad (1.d)$$

where R_L is the load resistance.

The conversion ratio of the ZVS-QR boost converter can be obtained, as in the case of the ZVS-QR buck converter in [18]:

$$M = \frac{1}{\frac{f_s}{2 \cdot \pi \cdot f_0} \cdot \varphi(Q, \alpha, M)} \quad (2.a)$$

with:

$$\varphi(Q, \alpha, M) = \alpha + \frac{Q}{2 \cdot M} + \frac{M}{Q} \cdot (1 - \cos\alpha) \quad (2.b)$$

where:

$$\alpha = \pi + \arcsin\left(\frac{Q}{M}\right) \quad (2.c)$$

To describe M as function of the control variable, the switching frequency f_s, it is necessary to use a numerical procedure. However it is possible a closed form solution, with some rearrangement of equation (2.a):

$$\frac{f_s}{f_0} = \frac{2 \cdot \pi \cdot (1 - M)}{\varphi(Q, \alpha, M)} \quad (3)$$

The regulation characteristic obtained from equation (3) shows that the load variation implies adjustments on the control variable to regulate the output voltage. This means that not only is necessary adjustments on control variable when the converter ratio varies but also when the load value changes. These changes could compromise the critical condition that guaranties zero-voltage switching, $M \geq Q$.

Designing ZVS-QR converters requires the design of the resonant circuit, the filter components and the power switches that includes the power MOSFET and the respective drivers. The design of the filter components is similar to that of the PWM converters, considering the minimum switching frequency.

2.2 Design Procedure for Boost Quasi-Resonant Converter

Typically, the design specifications for a CMOS dc-dc converter include: output voltage, V_O; input voltage range, $V_{I_{\min}}$ to $V_{I_{\max}}$; the load resistance range, $R_{L_{\min}}$ to $R_{L_{\max}}$; maximum switching frequency, $f_{S_{\max}}$. From the design specifications, the maximum and minimum value for the conversion ratio is given by:

$$M_{\min} = \frac{V_O}{V_{I_{\max}}} \quad (4.a) \qquad M_{\max} = \frac{V_O}{V_{I_{\min}}} \quad (4.b)$$

Considering the input voltage and load range the worst condition that could compromise the zero-voltage switching occurs for the minimum conversion ratio, $M_{\min}$, and maximum normalized load, $Q_{\max}$, defining a boundary condition described by equation (5).

$$\frac{V_O}{V_{I_{\max}}} \geq \frac{R_{L_{\max}}}{Z_0} \Leftrightarrow Z_0 \geq \frac{R_{L_{\max}}}{M_{\min}} \quad (5)$$

This situation will correspond to the maximum switching frequency, $f_{S_{\max}}$, given the minimum value for the characteristic impedance.

For the definition of the input voltage and load range the maximum voltage value that the NMOS MOSFET, acting as active switch, supports, must be taken into account. This aspect is fundamental when designing DC-DC converters in CMOS technology. The relation between the maximum value and the input voltage and load ranges will be given by:

$$V_{DSNMOS_{\max}} = V_O \cdot \left(1 + \frac{M_{\max}}{M_{\min}} \cdot \frac{R_{L_{\max}}}{R_{L_{\min}}}\right) \quad (6)$$

Equation (6) shows that even for fixed load and input voltage the maximum voltage on the active switch is twice the maximum voltage at the converter output. This will represent a problem if the output voltage is near the maximum CMOS process voltage, or for high load variations, especially if the switching frequency rises to tens or even hundred of MHz (although there is the possibility of producing high-voltage CMOS compatible transistors [19], these transistors operate at lower frequencies). The maximum current for the same transistor, in the worst case, can be obtained considering the maximum conversion ratio and the maximum load current.

$$I_{DNMOS_{\max}} = I_{L_{\max}} = M_{\max} \cdot I_{O_{\max}} \quad (7)$$

For the PMOS MOSFET, the maximum voltage stress and the maximum current stress will occur for $\alpha = \pi$.

$$V_{DSPMOS_{\max}} \cong -V_O \quad (8.a) \qquad I_{DPMOS_{\max}} = 2 \cdot M_{\max} \cdot I_{O_{\max}} \quad (8.b)$$

Considering the situation of maximum switching frequency, corresponding to $V_I = V_{I_{\max}}$ and $R_L = R_{L_{\max}}$, and that Z_0 assume the minimum value given by equation (5), equation (3) will be rewritten as:

$$\frac{f_{S_{\max}}}{f_0} = \frac{2 \cdot \pi}{M_{\min} \cdot \left[\frac{1}{2} + \alpha + (1 - \cos\alpha)\right]} \qquad (9)$$

In the situation of boundary condition $\alpha = \alpha_{\max} = \frac{3 \cdot \pi}{2}$ equation (9) simplifies to:

$$\frac{f_{S_{\max}}}{f_0} = \frac{4 \cdot \pi}{M_{\min} \cdot 3 \cdot (1 + \pi)} \cong \frac{1}{M_{\min}} \qquad (10)$$

The minimum switching frequency will be achieved when $V_I = V_{I_{\min}}$ and $R_L = R_{L_{\min}}$. In this way, equation (3) assumes a new form:

$$\frac{f_{S_{\min}}}{f_0} = \frac{2\ \pi}{M_{\max}\left(\frac{R_{L_{\min}}}{2}\frac{M_{\min}}{R_{L_{\max}}}\frac{M_{\max}}{M_{\max}} + \alpha_{\min} + \frac{R_{L_{\max}}}{R_{L_{\min}}}\frac{M_{\max}}{M_{\min}}(1 - \cos\alpha)\right)} \qquad (11.a)$$

with:

$$\alpha_{\min} = \pi + \operatorname{arcsen}\left(\frac{R_{L_{\min}} \cdot M_{\min}}{R_{L_{\max}} \cdot M_{\max}}\right) \qquad (11.b)$$

For CMOS integration the maximum switching frequency will assume particular importance, due to CMOS process limitations on frequency and converter efficiency optimization. In this way the maximum switching frequency must be chosen to meet the above requirements and will depend on the CMOS process in use. Resonant frequency, f_0, will be obtained after using equation (10). With the value of the resonant frequency and the characteristic impedance imposed by the boundary condition the resonant circuit components are given by the follow equations:

$$L_0 = \frac{Z_0}{2 \cdot \pi \cdot f_0} \quad (12.a) \qquad C_0 = \frac{1}{2 \cdot \pi \cdot f_0 \cdot Z_0} \quad (12.b)$$

An extension of the design method used for hard-switching converters for the design of the power switches and respective driver circuits, presented on [12], can be used for ZVS-QR converters.

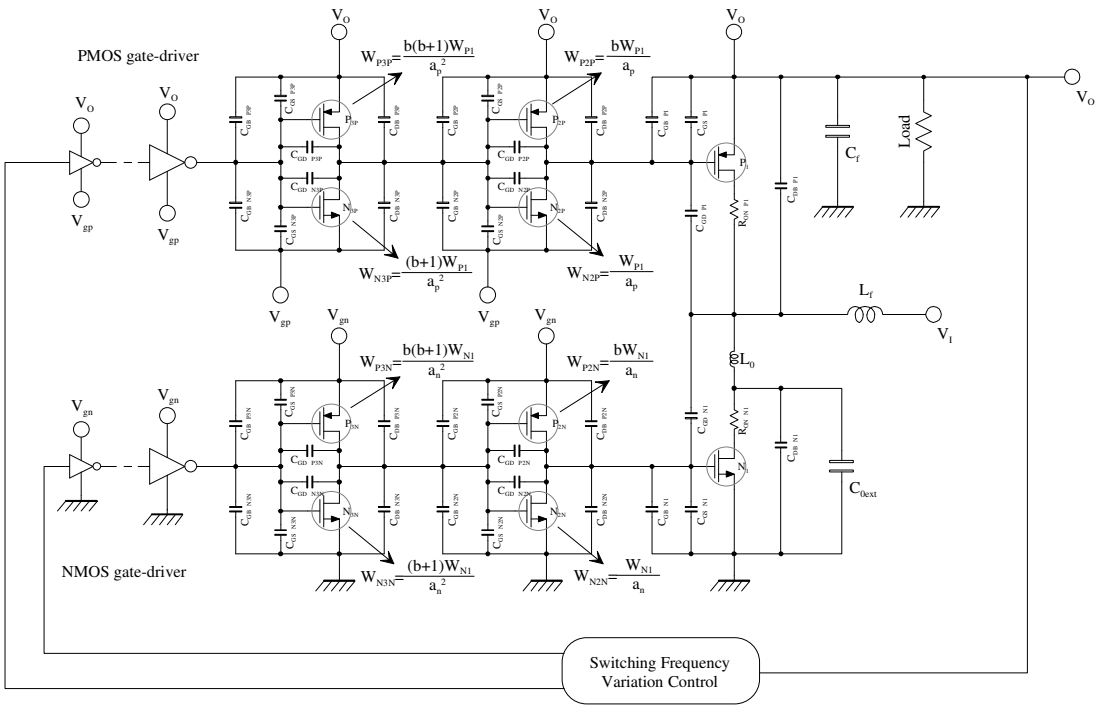

Fig. 2. ZVS-QR Boost converter model including parasitic impedances and transistor sizes.

2.3 Power Stage Loss Model

The power loss model is obtained considering the proposed method for buck hard-switching DC-DC converters on [12]. This method could be extended, with a few modifications on the power MOSFET and the respective drivers design model, for buck ZVS-QR dc-dc converters. A boost ZVS-QR converter model that includes the parasitic impedances is shown in Figure 2.

The losses of the driver circuit of the PMOS power device, P1, shown on Figure 2, are the same as for the buck hard-switching dc-dc converters, [12].

For the PMOS power transistor the energy associated to the switching losses per unit will be slightly different and given by:

$$E_{P1} = \left(C_{gb0PMOS} + C_{gs0PMOS} + C_{gd0PMOS}\right) \cdot \left(V_O - V_{gp}\right)^2 \quad (13)$$

Considering the contributions from the driver circuit and the power losses from the PMOS power transistor, the total power loss associated to P_1 is obtained from:

$$P_{P1TOTAL} = \frac{R_{0PMOS}}{W_{P1}} \cdot {i_{rmsPMOS}}^2 + W_{P1} \cdot E_{P1TOTALswitching} \cdot f_S$$

(14.a)

with:

$$E_{P1TOTALswitching} = E_{P1} + E_{PMOSdrivers} \quad (14.b)$$

Where R_{0PMOS} is the PMOS on resistance per unit length, W_{P1} is the P_1 width, f_s the switching frequency and $I_{rmsPMOS}$ the PMOS rms current.

For the NMOS transistor, N_1, and the respective driver circuit, similar equations are obtained:

$$P_{N1TOTAL} = \frac{R_{0NMOS}}{W_{N1}} \cdot {i_{rmsNMOS}}^2 + W_{N1} \cdot E_{N1TOTALswitching} \cdot f_S$$

(15.a)

with:

$$E_{N1TOTALswitching} = E_{N1} + E_{NMOSdrivers} \quad (15.b)$$

where:

$$E_{N1} = \left(C_{gb0NMOS} + C_{gs0NMOS} + C_{gd0NMOS}\right) \cdot {V_{gn}}^2 \quad (15.c)$$

From (14) and (15) it can be concluded that the conduction losses are proportional to the width of power MOSFET. In this way it is possible to optimize the losses on the power transistors and respective drivers, as in [12] for hard-switch converters.

For the definition of the tapering factor, t_f, it has to be consider the losses in the driver circuits, as in [12] for hard-switch converters, remaining the functional behaviour of the converter. So, a different solution based on [3] was used, where t_f is defined as five to ten times less than the charge of the resonant capacitor, C_0, corresponding to the first operating interval of ZVS-QR boost converter, the short time interval.

3 QUASI-SQUARE-WAVE CONVERTERS

As in the case of the QR Converters, the ZVS-QSW and ZCS-QSW converters are also obtained from conventional PWM (Pulse Width Modulation) with some additional reactive components, with a different circuit topology.

ZVS-QSW converters present lower voltage and higher current stress on the switching devices. On the other hand ZCS-QSW converters have lower current and higher voltage stress [20]. The ZVS-QSW topologies present the advantage of the addition of only one capacitor, when compared with the QR or ZCS-QSW topologies, because theoretically the additional inductor can be placed in parallel with the filter inductor. Thus, ZVS-QSW topologies appear as an alternative to the use of high-voltage transistors in ZVS-QR topologies. Another advantage is that the parasitic capacitors associated to the two power transistors are in parallel and contribute both to the resonant capacitor. However, it is necessary to take into account some drawbacks: the higher variation of the inductor current, which leads to an increase of the Electromagnetic Interference (EMI) when compared with the Quasi-Resonant topologies.

To obtain a QSW converter it is necessary to manipulate the low-frequency storage elements in the correspondent PWM topology, followed by the insertion of resonant tank elements. Certain PWM converters cannot be transformed into their corresponding ZVS-QSW or ZCS-QSW topologies, unless new low frequency storage elements are added to the original PWM converter (e.g. the ZCS buck converter) [20]. This solution is only attractive for the topologies that do not need the additional low-frequency elements, as the ZVS buck converter, presented in Figure 3.

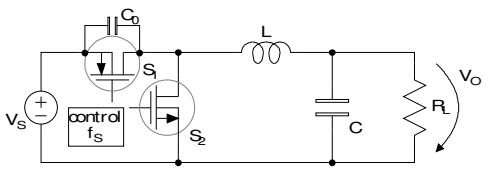

Fig. 3. Buck ZVS-QSW converter.

In this converter the output filter inductor is also used as the resonant inductor. Therefore, this solution appears more attractive then the correspondent QR topology, presented in Figure 1. b), since the resonant inductor is not present.

3.1 Buck Quasi-Square-Wave Converter Theoretical Operation

A detailed steady state analysis of the buck ZVS-QSW converter theoretical operation is presented in [20]. Using this steady state analysis and performing an energy balance for one operation period, considering no losses, it is possible to obtain a set of five equations which resolution is not trivial. In order to solve this problem, a semi closed method to obtain the conversion ratio for the design of a buck ZVS-QSW converter was developed in [21]. Using the result obtained in [21] the frequency conversion ratio is given by:

$$\frac{f_s}{f_0} = \frac{4 \cdot \pi \cdot M^2 \cdot (1-M)}{Q \cdot \left[\frac{M^2}{Q^2} \cdot \frac{{I_M}^2}{{I_L}^2} - (2 \cdot M - 1) \right]} \qquad (16)$$

Assuming that M is known and that the parameter Q is function of the load and of L_0, the only unknown variable is I_M (maximum current in the inductor). The ratio between the maximum and average currents in the inductor, $\alpha_{I_L} = I_M / I_L$, results from the solution of (17):

$$a \cdot {\alpha_{I_L}}^3 + b \cdot {\alpha_{I_L}}^2 + c \cdot \alpha_{I_L} + d = 0 \qquad (17)$$

where:

$$a = -\frac{1}{2 \cdot Q(1-M)} \qquad (17.a)$$

$$b = \frac{1}{Q} + \frac{M}{Q \cdot (1-M)} \qquad (17.b)$$

$$c = \arccos\left(\frac{M-1}{M}\right) + \frac{1}{1-M} \cdot \sqrt{2 \cdot M - 1} + \frac{(2 \cdot M - 1) \cdot Q}{2 \cdot M^2 \cdot (1-M)} \qquad (17.c)$$

$$d = M \cdot Q \qquad (17.d)$$

From equation (17) three solutions are obtained for α_{I_L}, but only one is in agreement with the normal behaviour of the converter. Substituting in (16) the valid α_{I_L} it is possible to obtain the conversion ratio, M, as function of the normalized switching frequency for different values of the normalized load, Q.

As in the ZVS-QR boost converter the load variation implies adjustments on the control variable to regulate the converter output voltage. This variation forces a critical condition to guarantee the zero voltage switching in the ZVS-QSW converter. In this case, independently of the normalized load, $M \geq 0.5$. Nevertheless, a design procedure is needed to design a ZVS-QSW buck converter in CMOS technology. The zero voltage switching critical condition implies the limitation of these converters to applications where the conversion ratio is above 0.5.

Designing ZVS-QSW converters have the same requirements as in the ZVS-QR converters. It is necessary to design the resonant circuit, the filter components and the power switches that include the power MOSFET and the respective drivers. Because of that a new design procedure is developed for CMOS ZVS-QSW converters in the next section.

3.2 Design Procedure for Buck Quasi-Square-Wave Converter

Some authors have proposed design methods for ZVS-QSW converters, [22]. However these methods are not appropriated for CMOS integration. A new proposal was made in [21] but without the design procedure for the power stage. In this way a more detailed and improved method is proposed in this paper.

The CMOS monolithic integration of ZVS-QSW converter implies a careful attention over the definition of circuit parameters. As a matter of fact the linear approximation made to obtain equation (16), is only valid if the normalized switching frequency is low [21]. This implies that Q should have the smallest value as possible (from equation (16)). Considering all the dependencies of Q, including the switching frequency, the load and

characteristic impedance Z_0, and taking into account the parameters of the CMOS process, the following design method is proposed:

1. Define the normalized load, Q, that with the conversion relation, M, of the converter to be designed, corresponds to a small ratio between the switching frequency and the resonant frequency.

2. With Q defined, obtain the characteristic impedance, Z_0, considering the maximum load resistance, $R_{L_{\max}}$, corresponding to the boundary condition. Obtain the ratio between I_M and I_L using equation (17). Determine the ratio between the maximum switching frequency, $f_{S_{\max}}$, and the resonant frequency using equation (16).

3. Design the power transistors and associated drivers using an extension of the method used in [12], function of the load current, I_O, and the maximum switching frequency, $f_{S_{\max}}$, which is defined considering the compromise between the occupied area and the converter efficiency, taking into account the limitations inherent to the specific CMOS process. Obtain the resonant frequency with the information of step 2.

4. Obtain the intrinsic parasitic capacitors of the power transistors that contribute to the resonant capacitor, C_0. The sum of these capacitances must be smaller than the resonant capacitor determined after steps 2 and 3. If not, return to step 1 and relax the specification of Q.

With this method it is possible to guarantee a normal behaviour of the converter in the worst case, defining as in the case of the ZVS-QR converters, ranges of variation for the input voltage and output load.
After the definition of the maximum normalized load, $Q_{\max}$, the characteristic impedance could be obtained by:

$$Z_0 = \frac{R_{L_{\max}}}{Q_{\max}} \tag{18}$$

Using equations (16) and (17) and considering the situation of $M_{\min}$, it is possible to obtain the values corresponding to the situation of maximum switching frequency, the worst condition to validate the restriction on the ratio between the switching and resonant frequencies. Using the same equations and making $M = M_{\max}$ and $Q = R_{L_{\min}} / Z_0$ it is possible to obtain the relation between the minimum switching and resonant frequencies, defining in this way the operating interval of the converter, as function of the ranges of the input voltage and of the load.
In the ZVS-QSW buck converter the filter inductor is shunted by the resonant inductor. So, the design of the filter components is reduced to the design of the filter capacitor. The filter capacitor value is obtained in a similar way as for the PWM converters considering the minimal switching frequency operation and assuming a ripple current on the inductor given by half of I_M:

$$\Delta i_L \cong \frac{I_M}{2} \tag{19}$$

The efficiency analysis of the converter is measured considering the situation of maximum switching frequency (with $Q_{\max}$ and $M_{\min}$), corresponding to the worst case for dynamical losses on the power stage.

3.3 Power Stage Loss Model

The power losses model of the power transistors and respective driver circuits is similar to the power loss model obtained for the ZVS-QR boost converter. The losses on the ZVS-QSW buck converter are characterized in the same way as for the ZVS-QR boost converter. The parasitic capacitances considered are the same because of the zero voltage switching. In this way, the equations from (13) to (15) are valid and can be applied.
For the definition of the tapering factor, t_f, the solution adopted is the same as in de ZVS-QR boost converter.

4 DESIGN PROCEDURES VALIDATION

This section presents simulation results of a ZVS-QR boost converter and a ZVS-QSW buck converter that validates the design procedures proposed in this work.

The ZVS-QR boost converter was design for the following specifications: $V_I = [1.08 \cdots 1.32]\text{V}$, $V_O = 3.3\text{V}$, $I_O = [9 \cdots 10]\text{mA}$, $\Delta i_L = 0.1 \cdot I_L$ and ripple output voltage below 1%. Taken as reference a maximum theoretical efficiency of 80% the maximum switching frequency for the CMOS

process is 100MHz. With that value and using the design methodology exposed in section 2, the parameters obtained for the converter are: L_0 = 90nH, C_0 = 4.18pF, L_f = 2.9µH, C_f = 1.9nF. The optimized transistors dimensions are W_{NMOS} = 339.6µm, W_{PMOS} = 552.9µm with $L_{NMOS} = L_{PMOS}$ = 1µm. The resonant capacitor will be formed by a NMOS parasitic capacitor and an additional shunt capacitor.

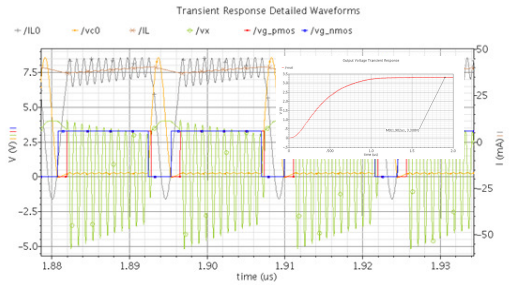

Fig. 4. Transient Analysis detailed Waveforms of output voltage (vout), inductors currents (IL and IL0), power transistors control signals (vg_nmos and vg_pmos) and resonant capacitor voltage (vc0) of the boost QR converter. Output voltage full transient response waveform.

The waveforms presented in Figure 4 shows some drawbacks on the use of ZVS-QR converters for integration purpose. The current in the resonant inductor and the voltage in the resonant capacitor oscillate in the last interval of the switching period. The parasitic resonance results from the accumulated energy in the PMOS parasitic capacitance, C_{gd}, when acting as the switching transistor. The accumulated energy is injected in a resonant circuit formed by the resonant inductor, L_0, and the capacitor resulting from the sum of C_{gd} with C_{db} in the PMOS power transistor. This resonance will be described by the following equations:

$$i_{L_0}(t) = \frac{V_\sigma}{Z_{0_P}} \cdot \text{sen}(\omega_0 \cdot (t - t_3)) + I_L \qquad (20.a)$$

$$v_{C_P} = V_\sigma \cdot \cos(\omega_0 \cdot (t - t_3)) - V_O \qquad (20.b)$$

where V_σ represents the C_{gd} accumulated energy resultant voltage, V_{C_P} represents the voltage in the PMOS total parasitic capacitance, the sum of C_{gd} with C_{db}, and Z_{0_P} represents the characteristic impedance of the parasitic resonance circuit.

This parasitic resonance causes a resonant voltage on the PMOS drain that presents a high voltage stress, not supported by the CMOS process. This imposes the use of a high voltage PMOS transistor. The other solution could be the use of a diode in the PMOS place, like in the discrete implementation, but it will lead to less efficiency. This will be a significant drawback in the use of ZVS-QR topologies for CMOS integration.

Using the section 3 design procedure, a ZVS-QSW buck converter was designed with the following characteristics: $V_I = [4.8 \cdots 5.2]\text{V}$, $V_O = 3.3\text{V}$, $I_O = 30\text{mA}$, $\Delta v_O = 0.05 \cdot V_O$, L_0 = 249nH, C_0 = 1.3pF, C_f = 990pF, $f_{S_{\max}} = 70\text{MHz}$. The optimized transistors dimensions were W_{NMOS} = 238.1µm, W_{PMOS} = 653.9µm with $L_{NMOS} = L_{PMOS}$ = 1µm.

The waveforms presented in Figure 5 are in good agreement with the expected results. After the transient, the converter tends to stabilize at the desired values for output voltage and average inductor current.

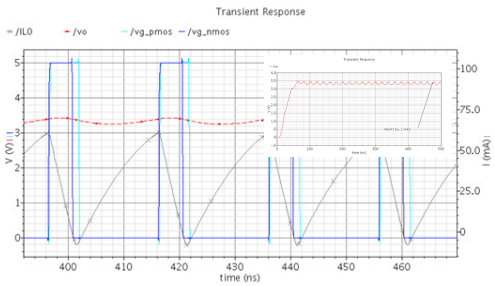

Fig. 5. Transient Analysis detailed Waveforms of inductor current, L0, output voltage, vo and PMOS and NMOS control signals. Output voltage full transient response waveform.

The theoretically efficiency, considering only the losses of the power transistors, is approximately 80%. The value obtained for the efficiency in the simulated circuit was about 7% less. The difference obtained is mostly caused by the overlap conduction on the inverters of the power transistors driver circuits.

5 CONCLUSIONS

Two design procedures for the implementation of resonant switching converters in CMOS technology are introduced. A ZVS-QR boost converter and a ZVS-QSW buck converter were conceived using the proposed design methods. The results obtained show a validation of the proposed design methodologies. Some drawbacks for the implementation of the ZVS-QR converters in CMOS are revealed for the initial assumptions considered. The use of high-voltage PMOS transistors is proposed to solve these

drawbacks. Nevertheless the parasitic resonance could cause a higher EMI.

The results obtained from the ZVS-QSW buck converter encourage this solution. The introduction of non-overlap circuits in the last inverters of the inverters chain of the power transistors driver circuits could reduce the switching losses.

The parasitic resonance in the CMOS integrated ZVS-QR converter reduce the advantage of lower EMI when compared with the CMOS integrated ZVS-QSW converter. In this context the utilization of CMOS integrated ZVS-QR converters will be conditioning to the study of solutions to reduce the parasitic resonance.

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