i-ETC: ISEL Academic Journal of Electronics, Telecommunications and Computers
CETC2011 Issue, Vol. 2, n. 1 (2013) ID-11

MULTI-STAGE MIXED FREQUENCY-TIME SIMULATOR FOR BANDPASS SAMPLING RECEIVER FRONT-ENDS

Pedro Miguel Cruz and Nuno Borges Carvalho
Instituto de Telecomunicações – Universidade de Aveiro
Departamento de Electrónica, Telecomunicações e Informática, Aveiro, Portugal
pcruz@av.it.pt nbcarvalho@ua.pt

Mikko E. Valkama
Tampere University of Technology, Tampere, Finland
mikko.e.valkama@tut.fi

Keywords: Band-pass sampling, Mixed-domain simulator, Software defined radio, Wideband receiver.

Abstract: This paper address the implementation of a mixed-domain simulator for first-order band-pass sampling receivers, which is based on an initial frequency-domain signal treatment followed by a time-domain simulation scheme. One of the proposed applications for this type of receivers is to perform the spectrum sensing feature, which is required in actual and future cognitive radio approaches. Some details about the multi-stage modelling strategy will be given focusing in each specific component of the receiver, wherein it is considered a mixed frequency-time signal treatment. Moreover, it will be summarized the main features of the implemented simulator, as well as potential improvements. Finally, several simulation examples obtained with the implemented simulator will be shown, in which are included the impact of a CW signal excitation in a received modulated signal and a multi-carrier signal reception scenario.

1 INTRODUCTION

The constant appearance of new communication standards (e.g. GSM, IEEE 802.11a/b/g/n, UMTS, WiMax, LTE, LTE-advanced) are imposing rough challenges to the wireless communication industry, either by the difficulty of integration of several standards in the same device or due to the incompatibility between each other in the different parts of the world. One of the most promising solutions for this contradictory situation is the deployment of software defined radio (SDR) [1] and cognitive radio (CR) [2] technologies, which demonstrate flexibility and agility in order to change carrier frequency, bandwidth, modulation format and transmitted power, but at the same time, respecting all the regulation for traditional radio transmitters maintaining a high energy efficiency as possible.

A possible receiver architecture solution to the design of agile SDR/CR radios is the band-pass sampling receiver (BPSR), [2 - 4], which due to the constant advancements achieved in the analogue-to-digital converter (ADC) technology is becoming an attractive receiver scheme, Figure 1.

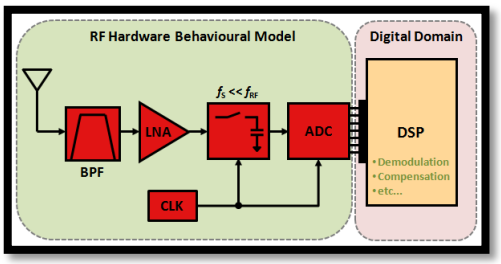

Figure 1: Band-pass sampling receiver block diagram.

The BPSR architecture (Figure 1) is constituted by an initial tuneable filter (BPF) or a bank of filters, then the incoming signal is amplified by a wideband low-noise amplifier (LNA), and afterwards it is converted to the digital domain by using a sample and hold (S/H) circuit followed by an ADC (frequently S/H and ADC components are integrated in the same chip). Finally, the incoming signal can be digitally processed taking advantage of digital signal processing to alleviate some mismatches of the analogue radio front end. In this sense, the main focus of this paper is to present a suitable simulator for this kind of complex design.

In this way, the proposed strategy uses a multi-stage approach to model the entire receiver chain considering independent models for each component (BPF, LNA, ADC, etc.). The developed simulator is able to represent the static behaviour of the complete receiver over its entire input bandwidth and under completely different input powers when excited by up to two different excitation signals.

Thus, in Section 2, we start by giving several details about the models used for each component of the BPSR taking into account its most important attributes as, for instance, the particular band-pass sampling behaviour and the respective mixer-free down-conversion to the first Nyquist zone (NZ), as well as the increase of the noise floor due to thermal noise effects of the LNA conjugated with clock and internal circuit sampling jitter. Then, Section 3 exemplifies a few facilities already implemented in the simulator and other that can be later on developed. In Section 4, it will be shown the simulator functionality by giving several results of a modulated signal when interfered by a sinusoidal signal, which is varied in power and carrier frequency. Moreover, the evaluation of a multi-carrier signal reception will also be a case of study. Finally, some conclusions will be drawn.

2 DETAILS ON THE MODELS

The fundamental concept of the BPSR is to design a receiving system with a reduced number of components taking advantage of the digital signal processing capabilities to achieve the required performance.

A fundamental necessity for this simulator is to allow the inclusion of measured data within the simulation environment. Based on this fact all the designed models are mostly based in laboratory measurements from real components. In the following it will be explained the major details about each specific component model.

2.1 Filtering Stage

Concerning on the filter component, if a static filter made of non-semiconductor devices is considered, it can be assumed linear unless some passive intermodulation (PIM) is detected, [5]. This element is not considered in the developed model. In that way, the filter modelling can be characterized just by the measured frequency-domain S-parameters (for a certain low input power) performed with the help of a network analyser within the entire input bandwidth desired to evaluate.

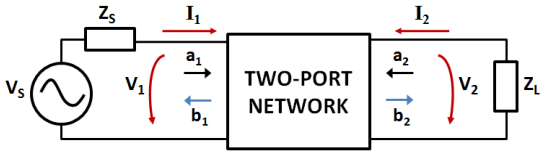

Figure 2: Two-port network showing incident (a_1, a_2) and reflected (b_1, b_2) waves used in S-parameters definition.

Thus, considering the simple 2-port network shown in Figure 2, the equations that describe the network are:

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases} \quad (1)$$

Afterwards, these formulas are used to calculate the time-domain signal waveforms at the output of the utilized filter through an inverse fast Fourier transform (IFFT). As well the reflection coefficients, both at input and output ports, are also being employed to determine impairments under non-50Ω sources or loads application.

In addition, to match the frequency grid being used in the simulations, it will be necessary to interpolate and/or extrapolate the measured S-parameters values due to the limited number of points provided by the network analyzer (instrument used to measure the S-parameters).

This happens because in the commercially available network analysers it is only possible to measure frequency-domain S-parameters between a limited range of frequencies (F_L to F_H in Figure 3), in which it is common to fail frequencies close to DC. In this way, in our models the values of the S-parameters between DC and the lower measurable frequency (F_L) have been linearly extrapolated.

Moreover, in Figure 3 it is shown the processing scheme that is necessary to be employed in the measured S-parameters. Here, it is assumed that measured frequency response is hermitian, i.e., the negative frequency response can be considered as the conjugate of the positive frequency response.

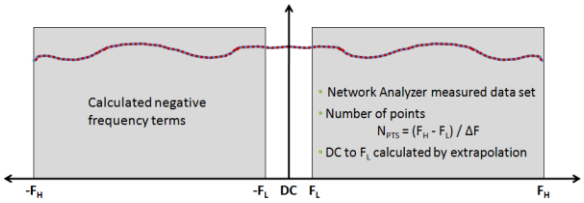

Figure 3: Processing scheme employed in the frequency-domain measured S-parameters to produce a time-domain output through an inverse FFT.

After that, the calculated frequency-domain signal is converted to a time-domain version by means of an IFFT, allowing the application of the subsequent nonlinear parts in the time-domain.

It should be referred that a similar reasoning will be applied in the succeeding component models.

2.2 Low-Noise Amplifier Stage

Regarding the second component (LNA) much has been written about nonlinear distortion in such type of devices, for instance in [6].

In small-signal operation, nonlinear behavior is often approximated by a simple polynomial, for instance a Taylor series can be used when the device is memoryless. On the other hand, when in large-signal operation, the transistor starts to clip the output signal due to the fact that it will saturate and it can be approximated by a large-signal transfer function, often by a describing function approach [6, 7]. Besides from that nonlinear behavior it is also important to determine non-ideal adaptations to 50Ω sources and loads and thus, include into the model information about S-parameters characteristics.

As a result, taking into account the previous statements, the implemented model in the simulator considers a mixed-domain signal treatment. Firstly, the S-parameters of the device are measured with a common network analyzer for a given low input power, Figure 4. This information is accompanied by the measured noise figure (NF) over the entire frequency range necessary to be simulated, Figure 5. Afterwards, it is followed by a nonlinear behaviour (Figure 6) based on a power series, expression (2), which is defined based on the actual performance of the device for a certain input frequency.

$$y(t) = a_0 + a_1 x + a_2 x^2 + \ldots + a_n x^n \qquad (2)$$

Thus, in order to implement the previous sequence of functions there is the necessity to follow the following sequential steps:

- *Apply a Fourier transform (FFT) to the input signal (coming from the filter)*
- *Apply the normalized vector (complex values) of the measured S-parameters to the obtained frequency-domain signal*
- *Create a new variable of white Gaussian noise with a given level (input noise floor plus maximum noise figure of LNA) and filter this frequency-domain signal with the shape of the measured NF*
- *Add the noise and the input signal vectors*
- *Apply an IFFT on the previous signal to obtain the correspondent time-domain version*
- *Apply the nonlinear behaviour (in this case, a power series) to the previous signal*

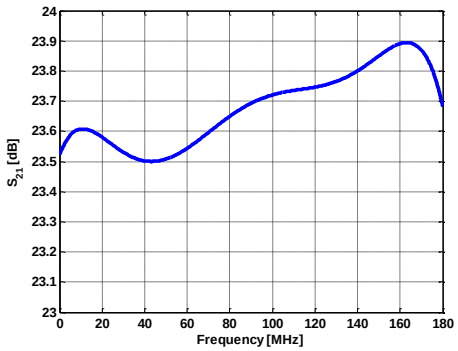

Figure 4: Measured forward transfer function (S_{21}) from the LNA within the bandwidth of interest.

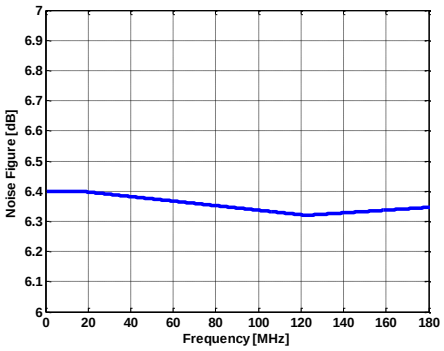

Figure 5: Measured noise figure for the LNA within the bandwidth of interest.

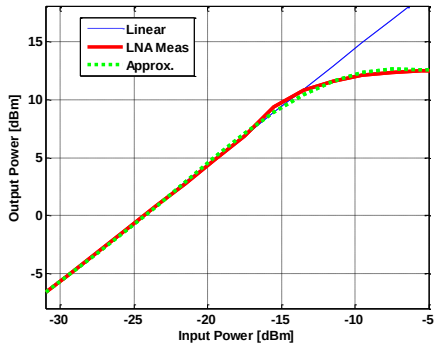

Figure 6: Measured LNA nonlinear characteristic for a low input frequency over imposed with the applied 5th-order Taylor polynomial approximation.

In future developments of this simulator the described model could be improved and make use of other much feasible options to model the nonlinearity of an LNA. For example, considering a device with memory, a Volterra series [8] analysis can be considered, since it will incorporate dynamic, baseband effects and thus approximating better the overall behaviour of the LNA mainly for small-signal. As well, if we are willing to cover small and large-signal operations, system-level models as X-parameters [9] should be considered.

2.3 Analogue-to-Digital Converter Stage

The last component to be modelled is the wideband S/H plus ADC, being in this specific component that resides the major innovation and significance to the developed BPSR simulator.

The new scheme employed to model the ADC component is proposed in [10] and shares a few similarities with the work presented in [11] for a sigma-delta ADC. In [10] it is proposed a system-level model composed of different independent blocks to characterize the entire behaviour of a wideband S/H plus ADC.

The first block is intended to describe the RF impairments of the input circuit, and account mainly for the RF mismatch. In radio frequency designs this mismatch and frequency characteristics can be expressed by the abovementioned S-parameters. These are mainly characterized by the mismatch loss (S_{11}) at the input matching circuit, which might demonstrate quite different performance with the frequency from the input to the output ports.

The second block will model the main non-ideal processes that occur in the sampling stage of the A/D conversion. In this block it is included the degradation of the signal-to-noise ratio (SNR) due to the aperture jitter of the sampling clock and ADC internal jitter, equation (3).

$$SNR_{dB} = -20 * \log_{10}\left(\frac{1}{2\pi . f_c . t_j}\right) \qquad (3)$$

Then, it is followed by a relevant block that performs the mechanism of band-pass sampling, i.e., folding back any input signal inside its bandwidth to the first Nyquist zone (NZ), as shown in Figure 7. Finally, a sub-block to model the complete nonlinear behaviour of the ADC is used, supported again in a power series approach.

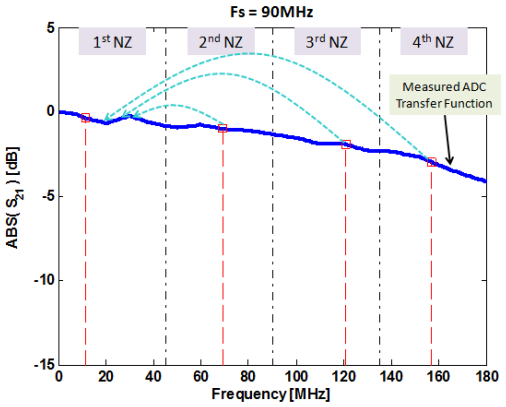

Figure 7: Measured transfer function characteristic (S_{21}) of the ADC, showing the concept of band-pass sampling within the first four Nyquist zones.

The ending block of the system-level model is the quantization segment that is designed to perform the conversion of the analogue sampled signal into an output digital word. This quantization phenomenon will originate a certain amount of quantization error, which can be represented by the value of the least significant bit (LSB). On the other side this LSB value is dependent on the reference voltage of the ADC and also on its number of bits. The mentioned quantization error will impose a certain SNR on the output signal, which is ideally approximated by the equation (4):

$$SNR_{dB} = 6.02 * N\_Bits + 1.76 \qquad (3)$$

Finally, all the blocks are interconnected and the input signal is treated based on a multi-stage mixed frequency-time scheme using a similar fashion as in the previous models.

3 SIMULATOR CAPABILITIES

In our vision this simulator will be interesting to be used as an educational tool, where it would make practical the development and evaluation of new compensation schemes for imperfections and impairments present in the receiving chain, allow the study of novel mitigation methods to overcome interference problems arising from a plenty of sources, and so on.

Looking to Figure 8 it is possible to observe the actual state of the implemented simulator. There it is seen a simulator constituted by four panels divided into an introductory panel, the configuration panel, the simulation results panel and the signal demodulation panel.

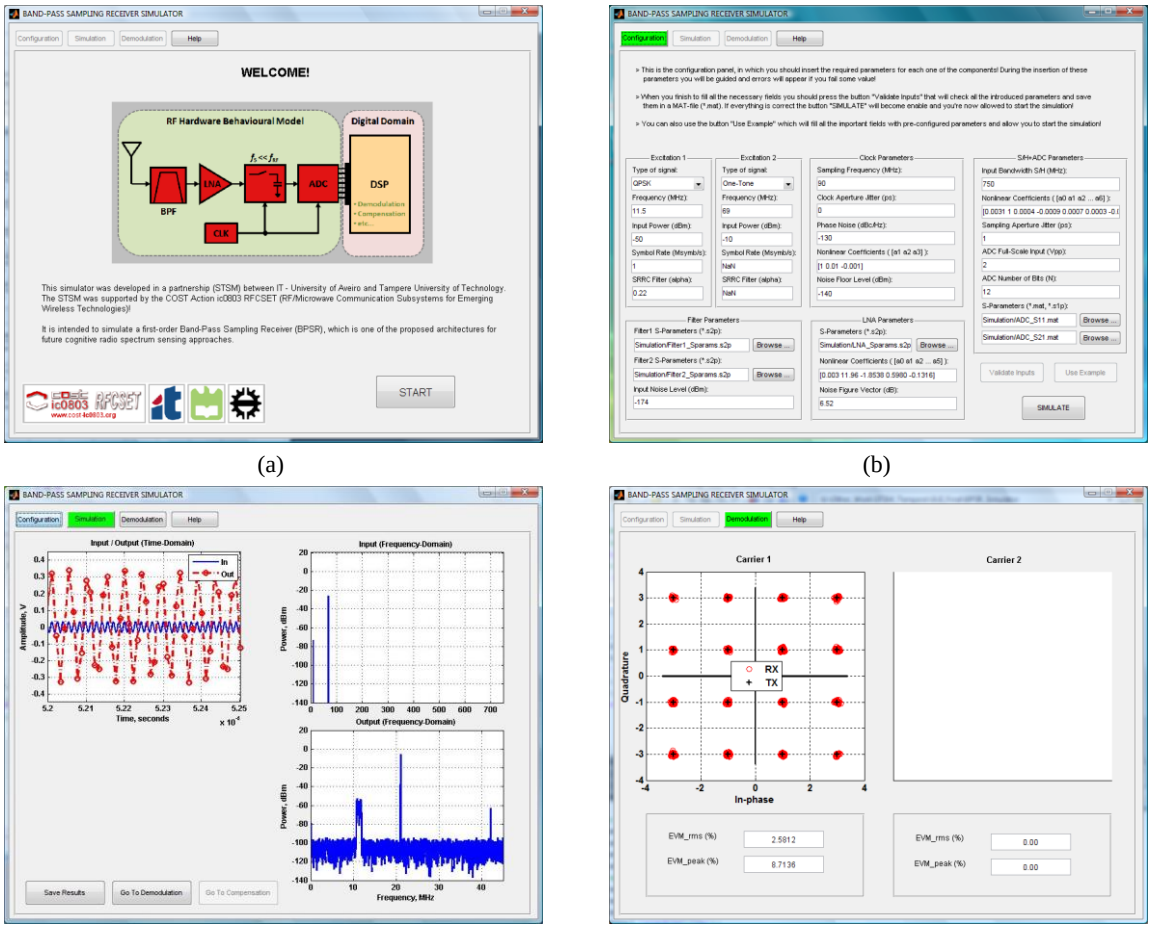

Figure 8: Illustrative appearance of the implemented simulator: (a) initial introductory panel, (b) configuration panel, (c) simulation results panel, and (d) signal demodulation panel.

The introductory panel is just the front cover for this simulator.

In the configuration panel the user should insert the required parameters for each component, being available the option to execute a pre-configured example.

The simulation results panel presents the input and output signals at both time and frequency domains, and is accompanied by a few more information regarding input and output powers, SNR values, etc., and has the functionality to save the obtained results into a file for further use.

Finally, the signal demodulation panel shows the results (constellation diagram and error vector magnitude) for the demodulation of the signals present at carrier one and two.

In summary, the most relevant features implemented in this simulator can be enumerated as follows:

- *Based on Matlab / Simulink but it is a simple executable program (*.exe)*
- *Several signal excitations are available (one-tone; multi-tone; QPSK; 16-QAM; 64-QAM) for one and/or two-channel operation*
- *Demodulation of I/Q modulated signals with Gain/Phase Compensation algorithm*
  - *EVM for signal in Channel-1 with an interference signal in Channel-2*
- *Multi-carrier operation allowing the signals to be band-pass sampled and demodulated*
- *Simple compensation scheme (Frequency Behaviour Compensation) devoted to minimize the multi-band and large bandwidth signals impairments*
  - *Correction of non-flat filter attenuation and non-ideal phase performance*

4 ILLUSTRATIVE SIMULATION RESULTS

In this section, it will be illustrated the functionality of the described multi-stage mixed-domain simulator by using a BPSR architecture, Figure 1, using data from real components.

Initially, it was considered that no band-pass filter is used to select the band to be received and thus, the entire simulated bandwidth is amplified in the LNA and folded back to the first NZ when being sampled at the ADC stage.

In that sense, the first configured component was an LNA that take values from a commercially available wideband (2 – 1200MHz) LNA, which has a 1dB compression point close to +11dBm, an approximated gain of 23dB, and a noise figure near to 6dB. This information can be seen in little detail in the low-noise amplifier section (2.2).

This was followed by a commercially 12-bit pipeline ADC that has a linear input range of around +10dBm (2Vpp) with an analogue input bandwidth (-3dB) of 157MHz, as can be merely understood in Figure 7. The ADC component has been sampled by a sinusoidal clock centred at 90MHz, with a constant noise floor and lower second and third harmonics.

Because of the used clock it was decided to simulate an input bandwidth of 180MHz in order to cover the first four NZ's (each one with 45MHz).

4.1 One-Tone Excitation

The first test to evaluate the performance of this simulator was to excite the previous described DUT with a sinusoidal (CW) signal centred in each NZ and then, study the attainable signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR).

In that way, we have determined those figures of merit when the signal power at the DUT input is varied from -80dBm to -8dBm with the results shown in Figure 9.

As can be seen the performance in the four NZ's is very similar for both SNR and SFDR values when operating in a small-signal region.

Moreover, observing the SNR results close to maximum input power is worst for higher frequencies (upper NZ's) due to ADC and sampling clock jitter accounted in the model, which will degrade the final SNR, see equation (3).

In addition, it is noted a sudden inversion in the SFDR curve for higher input powers due to the nonlinear distortion generated in the LNA and that surpasses the quantization noise level generated in the ADC component.

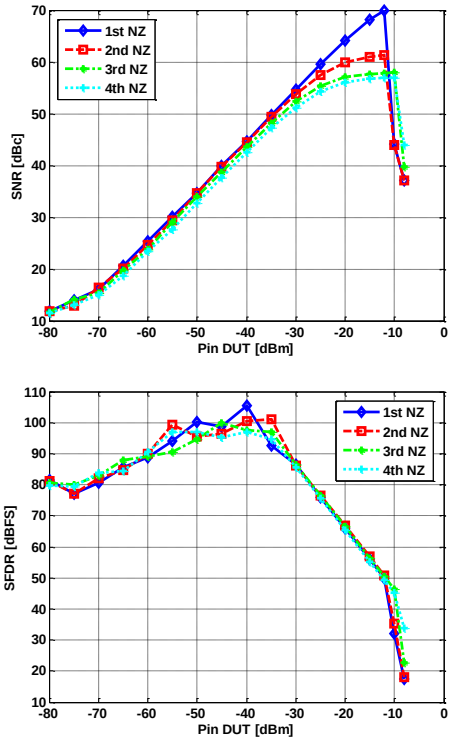

Figure 9: Obtained SNR (top) and SFDR (bottom) values for the BPSR design when evaluated at different NZ's.

4.2 Modulated Signal with CW Interference

The second test attempts to assess the impact of a CW interference in a QPSK and 16-QAM modulated signals when this interference is swept in power and varied in frequency. The spectra's for each situation is presented in Figure 10.

In this simulation we maintained the QPSK (symbol rate of 5Mbps) and 16-QAM (symbol rate of 6Mbps) signals in the 1st NZ (11.5MHz) with a fixed input power close to -40dBm. Regarding the CW interference it is put in the 2nd NZ, more precisely at 69MHz, for the power sweeping case. When varying its carrier frequency it is set to an input power of -20dBm.

The obtained results are illustrated in Figure 11, where it can be seen that a CW interference does not cause any issue to signal demodulation but except when it saturate the ADC device for an input of -10dBm. As regards to the CW frequency variation it will completely damage the signal demodulation when the input frequency is folded over the desired signal. These impacts can be also perceived in Figure 12 analyzing the constellation diagrams and spectra's.

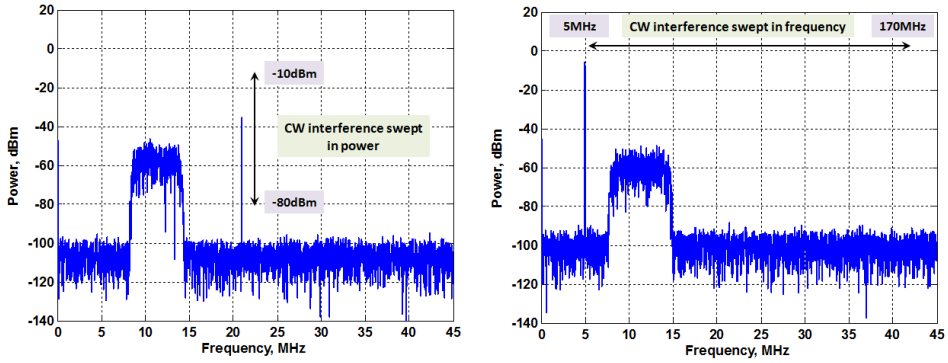

Figure 10: Spectrum of the QPSK/16-QAM signal with a CW interference when sweeping its input power (left) and varying its carrier frequency throughout the several NZ's (right).

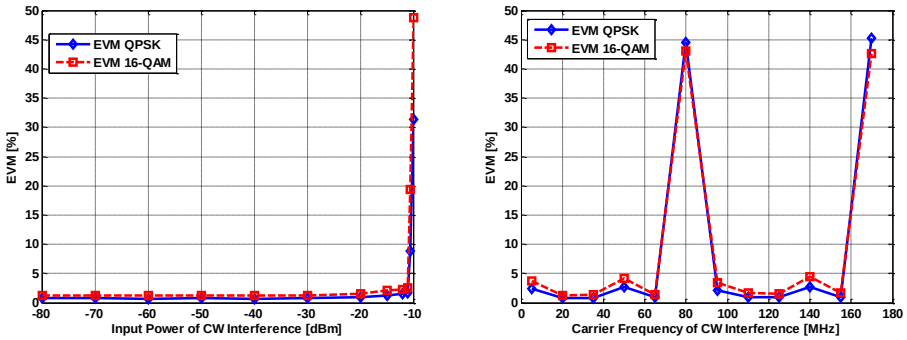

Figure 11: Error vector magnitude obtained for QPSK and 16-QAM modulated signals under CW interference: sweeping input power (left) and varying carrier frequency (right).

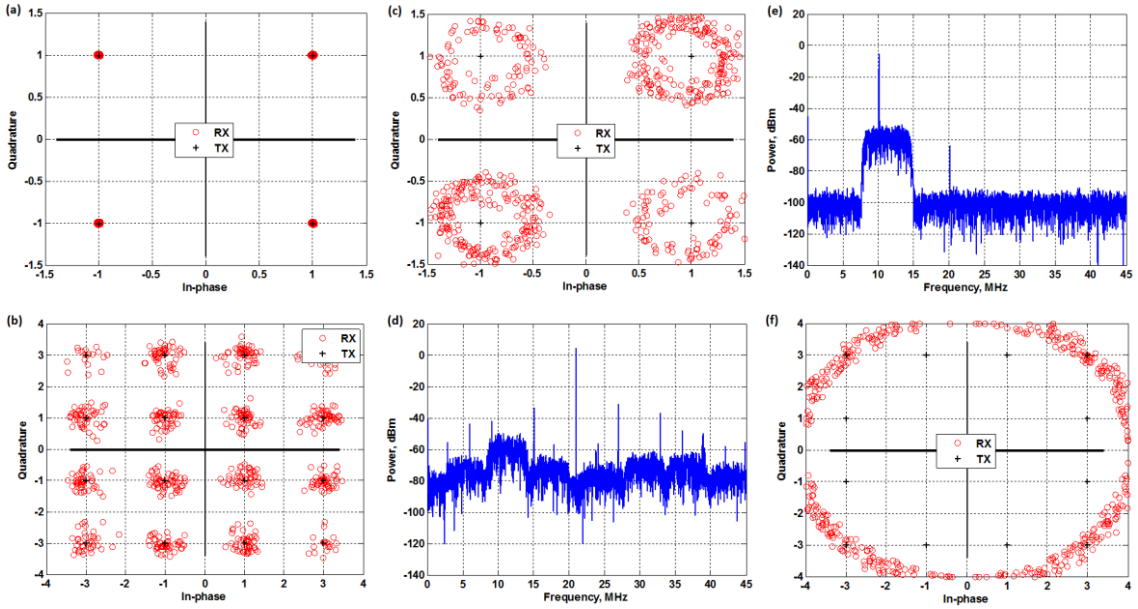

Figure 12: Results for CW power sweeping with constellation diagram at (a) -15dBm, (b) -11dBm, (c) -10dBm, and (d) spectra at -10dBm (fully clipped). Results for CW frequency variation with (e) spectra at f_{CW} = 80MHz being folded over the modulated signal and (f) respective constellation diagram.

4.3 Multi-Carrier Operation

The last test consists in the computation of the EVM for two modulated signals being simultaneously received. In this situation we have used a 16-QAM signal in channel one centred at 11.5MHZ (1st NZ) and carrying a symbol rate of 6Mbps. The channel two have a QPSK signal with 3Mbps of symbol rate and situated at 128MHz (3rd NZ) being directly folded back to 38MHz. The integrated power for channel one is -40dBm and for channel two is around -20dBm. The obtained constellation diagrams are shown in Figure 13 corresponding to an rms EVM of 3.99% for the 16-QAM signal and 0.41% for the QPSK signal.

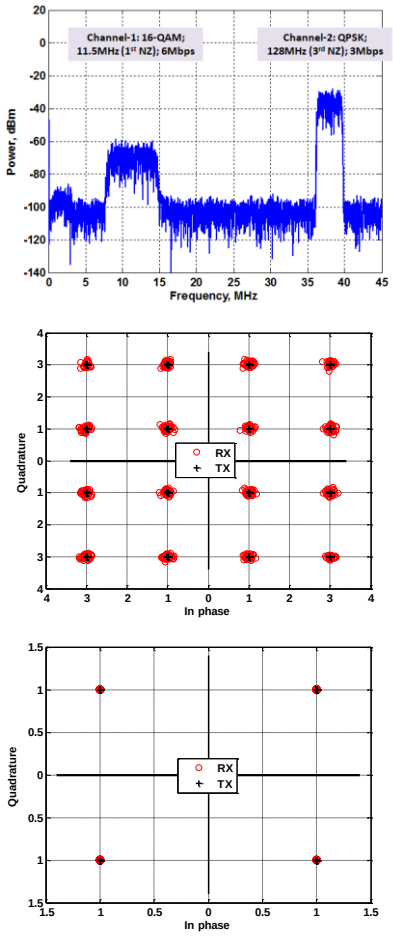

Figure 13: Spectra for the multi-channel operation case (top) and constellation diagrams obtained for 16-QAM signal (middle) and QPSK signal (bottom).

5 CONCLUSION

In this paper a different simulator approach for band-pass sampling receivers have been described in depth, which is based on a multi-stage mixed frequency-time design.

The presented simulator may become a valuable educational tool to evaluate the performance of such a type of receiving architectures that are intended for wideband SDR systems.

Several examples have been shown based in real-world scenarios and with the obtained results it is then possible to improve the overall signal reception by using several compensation and mitigation schemes, which may be implemented and tested on top of the provided simulator.

ACKNOWLEDGEMENT

The authors would like to acknowledge the support of this work within the COST Action IC0803 – RFCSET, and to thank Portuguese Science and Technology Foundation (FCT) for the PhD grant given to the first author (SFRH/BD/61527/2009).

REFERENCES

[1] Mitola, J., "The Software Radio Architecture", *IEEE Communications Magazine*, Vol. 33, no.5, pp. 26-38, May 1995.

[2] Vaughan, R., Scott, N., and White, D., "The Theory of Bandpass Sampling", *IEEE Trans. on Signal Processing*, Vol. 39, no. 9, pp. 1973-1984, Sept. 1991.

[3] Tseng, C. and Chou, S., "Direct Downconversion of Multiband RF Signals Using Bandpass Sampling", *IEEE Trans. on Wireless Communications*, Vol. 5, no. 1, pp. 72-76, Jan. 2006.

[4] Akos, D., Stockmaster, M., Tsui, J. and Caschera, J. "Direct Bandpass Sampling of Multiple Distinct RF Signals", *IEEE Trans. on Communications*, Vol. 47, no. 7, pp. 983-988, July 1999.

[5] Lui, P., "Passive Intermodulation Interference in Communications Systems," *Electronics & Communication Engineering Journal*, June 1990.

[6] Wambacq, P., and Sansen, W., "Distortion Analysis of Analog Integrated Circuits," *The Springer International Series in Engineering and Computer Science*, 1998.

[7] Pedro, J.C., and Carvalho, N.B., *Intermodulation Distortion in Microwave and Wireless Systems and Circuits*, Artech House, London, 2003.

[8] Schetzen, M., *The Volterra and Wiener Theories of Nonlinear Systems*, R. E. Krieger Publishing, 1989.

[9] Verspecht, J., and Root, D., "Polyharmonic Distortion Modeling," *IEEE Microwave Magazine*, Vol. 7, no.3, pp. 44-57, June 2006.

[10] Cruz, P.M., Carvalho, N.B., and Valkama, M., "Measurement-based Modelling of Analogue-to-Digital Converters under RF Impairments," under submission to *IET Circuits, Devices and Systems*.

[11] Brigati, S., Francesconi, F., Malcovati, P., Tonietto, D., Baschirotto, A., and Maloberti, F., "Modeling Sigma-Delta Modulator Non-Idealities in Simulink," *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, Vol. 2, pp. 384-387, July 1999.