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PLANAR CMOS AND MULTIGATE TRANSISTORS BASED WIDE-BAND OTA BUFFER AMPLIFIERS FOR HEAVY RESISTANCE LOAD *

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Abstract. *Analog buffer amplifier configurations capable of driving heavy resistive load using different operational transconductance amplifier (OTA) are presented in this paper. The OTA CMOS buffer configurations are designed using 0.18 µm SCL technology library in Cadence Virtuoso tool and multigate transistor OTA buffer in TCAD Sentaurus tool. CMOS OTA buffer configuration using simple OTA outperform the OTA buffer circuits using other OTAs in terms of power dissipation and stability. Measured results show that the OTA buffer circuit works well for resistive load below 100 Ω. The gain tuning of up to 5 V/V is achieved with RL equal to 50 Ω, output swing of 1 V. OTA buffer configuration implemented using multigate transistor with resistive load below 1 kΩ exhibits a bandwidth around 5 GHz and tunable gain up to 5 V/V.*

Key words: *OTA, buffer amplifier, resistive load, multigate transistor*

1. INTRODUCTION

The modern electronics systems are predominantly made up of digital circuits. However, every signal in nature is in analog form. In order to have a suitable interface with natural signals all the electronic systems need to have analog circuit based sub-modules. The fast growing demand for high speed and high frequency integrated circuits have motivated the researchers to design high performance analog circuits. Many applications require analog buffer amplifier capable of driving heavy resistive load (i.e. high load currents typically due to resistive loads less than 100 Ω) [1, 2]. In [2], OTA buffer amplifier configurations with high input dynamic range, wide-bandwidth, tunable gain, as well as with heavy load driving capability are proposed. The hardware implementation and

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testing of these CMOS OTA buffer configurations are presented in [1]. CMOS buffer amplifier in class AB configuration is commonly used to drive resistive load. Buffer amplifier configuration for driving heavy resistive load which are variants of class- AB theme are in literature [3-5].

Modern electronic gadgets have high speed processors which are implemented using the non-planar device structures instead of conventional planar transistors in which the analog part still uses CMOS design using planar transistors. Fabrication of the analog circuit and digital circuit for the same electronic system in two different process technologies results in high cost. Hence, this paper also focuses on realizing analog circuits in new process technology nodes.

Digital circuits fabricated using the scaled-down new transistors are reported in literature [6-16]. Compared to the digital design, analog circuit design is more sensitive to the device parameters. In scaled down devices, nonlinearities that dominate can affect the circuit design. As the device dimension reduces, the design complexity increases in analog circuit design compared to the digital circuit design. The digital circuits have already switched to the nano-scale regime. Research on analog circuit design using scaled down device architectures is still going on [7-11]. Among the multigate transistors, gate-all-around FET (GAAFET) is a device with better gate control over the channel which can be scaled down below 5 nm. Another multigate device is reconfigurable field-effect transistor (RFET) that can be configured as an n-type FET or a p-type FET by applying an appropriate bias. RFET device structures with triple gate, double gate and single gate are reported in the literature [9-12]. Among these RFET devices, single gate RFET (SG-RFET) is a simple device which has the structure similar to GAAFET device. Analog and digital circuits designed using SG-RFET and GAAFET devices can give an insight to the design possibilities in nanoscale implementation. The OTA buffer amplifier configurations discussed in [2] implemented using SG-RFET OTA and GAAFET OTA are presented in [7].

In this paper, the comparison of OTA buffer configurations implemented using different CMOS OTA and also using different non-planar device OTA topologies are presented. The performance of OTA buffer configurations proposed in [2] implemented using different CMOS configurations are demonstrated. To the best of our understanding this kind of work is for the first time in literature. The experimental results of the OTA buffer configurations fabricated using simple OTA are compared with the theoretical results which are explained in detail in the results and discussion section. The logic circuits implemented using different RFET devices are presented in [15] in which the logical effort of the logic gates using RFET is low compared to the CMOS based design. The low propagation delay due to the reduced parasitic capacitance makes this RFET device outperform the conventional transistors. As the analog circuits using RFET devices are not reported in literature, we have demonstrated the OTA buffer configurations using non-planar transistor OTA- SG-RFET OTA and GAAFET OTA to analyse the possibilities of non-planar transistors in analog circuit design. The electrical characterization of the SG-RFET, GAAFET device and the circuits based on that are presented in [7] and [8] which is used in this work for the buffer configuration implementation.

The implementation of CMOS OTA buffer configurations has been carried out in Cadence virtuoso tool in 0.18 µm technology node and the implementation of multi-gate OTA buffer configurations in 2D TCAD Sentaurus tool. The organization of the paper is as follows: In section 2, OTA buffer amplifier architectures, CMOS OTA topologies and multigate transistors are presented. Section 3 is about results and discussions followed by conclusion in section 4.

2. Implementation of OTA Buffer Configurations

Analog buffer amplifier using OTA is shown in Fig. 1 which is named buffer configuration 1 in [2]. N-stage unity gain and tunable gain OTA buffer circuit named as buffer configuration 2 and buffer configuration 3 respectively are presented in [2]. Buffer configuration 1 uses a single OTA with voltage series feedback as shown in Fig. 1. The open loop OTA has high output impedance. To obtain heavy resistance load driving capability, the output impedance of open loop OTA can be reduced by connecting OTA in a voltage series feedback configuration. The output impedance of buffer configuration 1 is dependent on the g_m of OTA. Hence, for increasing load drive capability and to obtain gain nearer to unity, g_m of OTA can be increased which in turn increases power dissipation.

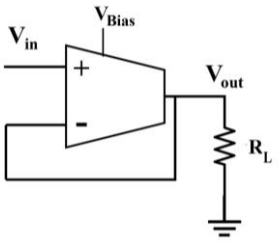


Fig. 1 Buffer configuration 1

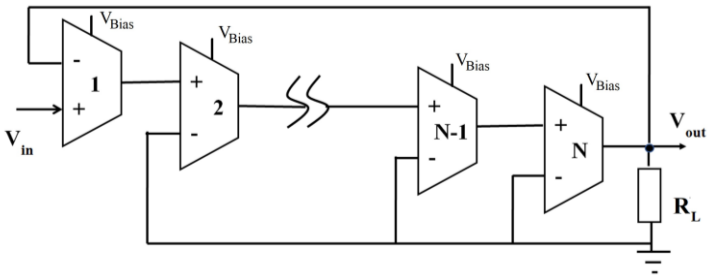


Fig. 2 N-stage Buffer configuration 2

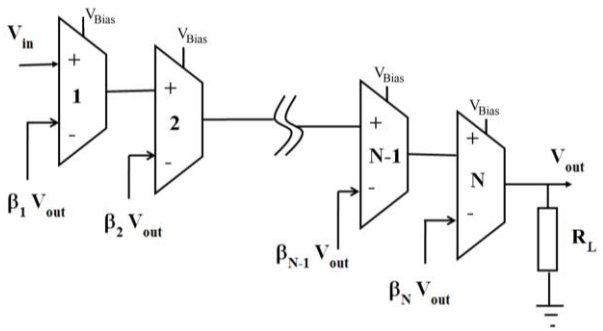


Fig. 3 N-stage Buffer configuration 3

In N-stage buffer configuration 2, the feedback to the OTAs except first stage is zero, i.e. the negative terminal of OTA is connected to AC ground. This results in the non-uniform differential voltage swing at the input of each OTA in the N-stage buffer, configuration 2. Figure 2 shows N-stage buffer configuration 2. N-stage tunable gain "non-inverting type" buffer configuration 3 [2] is shown in Fig. 3. The output impedance of N-stage buffer configuration 3 is low compared to buffer configuration 1 and N-stage buffer configuration 2 configuration. Furthermore, the gain is dependent on the feedback factor β_1 of the N-stage buffer configuration 3. By varying the feedback voltage of the first stage ($\beta_1 V_{out}$), the gain can be varied which makes the OTA buffer configuration to function as a tunable gain buffer amplifier configuration. The OTA block can be selected or designed according to the area of application.

2.1 CMOS OTA topologies

A variety of single ended output CMOS OTA topologies have been reported in literature [17-19]. Among these OTA topologies, four OTA topologies, namely simple OTA, folded cascode OTA (FC-OTA), recycled folded cascode OTA (RFC-OTA) and Nauta's OTA, are considered in the buffer design for driving resistive load. Other OTA topologies have very high DC voltage gain which is not used for the OTA buffer design due to its reduced bandwidth. Fig. 4 (a) depicts the simple OTA where the voltage gain of the first stage is almost unity. Hence the overall DC voltage gain depends on the second stage which is not very high. Fig. 4 (b) and 5 (a) represent the FC-OTA and RFC OTA configurations respectively with DC voltage gain less than 60 dB. Fig. 5 (b) represents the Nauta's OTA using inverters. Simple OTA, FC-OTA, RFC-OTA and Nauta's OTA are designed and implemented in Cadence virtuoso tool with SCL 0.18 µm library. Table 1 presents the parameters of different CMOS OTAs implemented in 0.18 µm technology node. OTA circuit designed using non-planar device (multgate transistors) are discussed in the next section.

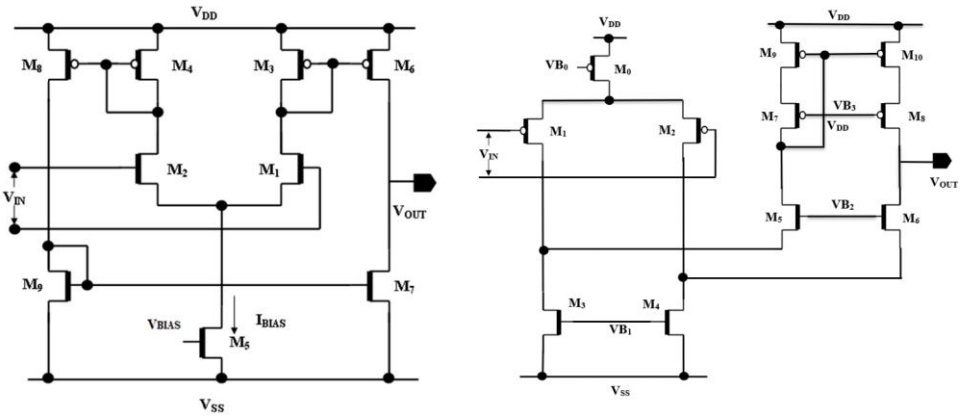
Table 1 Parameters of CMOS OTA configurations

Parameters	CMOS OTA Types			
	Recycled Folded cascode OTA (RFC-OTA)	Folded Cascode (FC-OTA)	Simple OTA	Nauta's OTA
Technology node (nm)	180	180	180	180
Supply Voltage (V)	±0.9	±0.9	±0.9	±0.9
R_L (kΩ)	100	100	100	100
Gain (dB)	56	48	28	35
GBW (MHz)	55	18	6000	6500
g_m (mS)	7.5	6	5	5

2.2 Multigate transistors

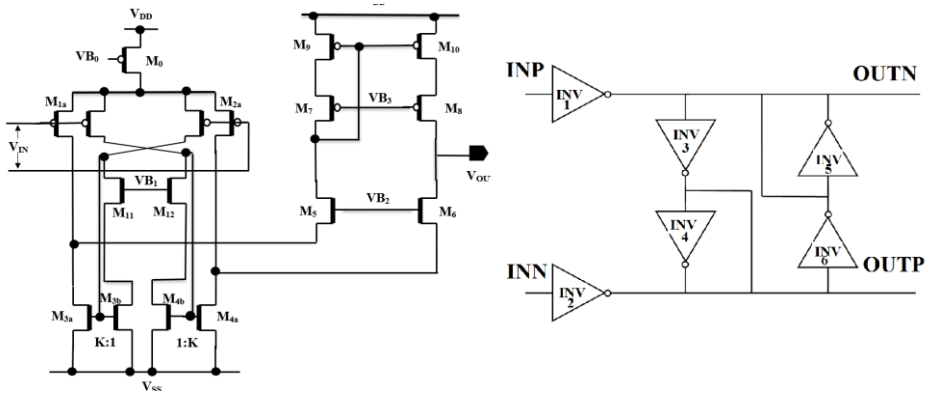
The demand for minimization has forced a significant downscaling in the physical size of devices. As device dimension shrinks, gate control over the channel of planar transistors becomes more difficult. New device architectures such as multi-gate devices, carbon nanotubes, tunnel FETs, single-electron devices, reconfigurable FETs, can outperform the conventional planar transistors in terms of speed, area and power consumption [9-16].

Among these devices, reconfigurable field-effect transistor (RFET) is an emerging multi-gate device which can be configured as an n-type FET or a p-type FET by applying an appropriate bias to the terminals. Fabrication of the RFET device is less complex compared to the existing MOS transistors, as there is no need for doping. RFET device structures with triple gate, double gate and single gate are reported in literature.



(a) (b)

Fig. 4 (a) Simple OTA (b) Folded cascode OTA (FC-OTA)



(a) (b)

Fig. 5 (a) Recycled Folded cascode OTA (RFC-OTA) (b) Bram's Nauta OTA

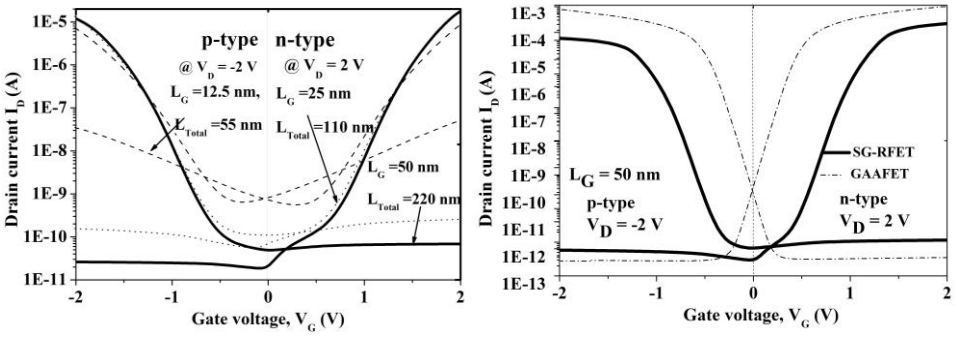
A simple and high-performance RFET with a single control gate RFET (SG-RFET) is proposed in [11]. Compared to triple gate RFET and polarity gate RFET, SG-RFET has a very simple structure.

The structure of SG-RFET device is similar to the multigate device gate-all-around FET (GAAFET). Fig. 6 (a) and (b) show the device structure of SG-RFET and GAAFET. In GAAFET, the gate material extends to surround the channel on all sides in order to attain maximum electrostatic integrity. Cylindrical type GAAFET offers the lowest

natural length which leads to further scaling of the device. The electrical characterization of SG-RFET and GAAFET and the OTA buffer circuit using SG-RFET OTA and GAAFET OTA are presented in [7,8]. Fig. 7 (a) [7,16] depicts the I_D- V_G characteristics of the SG-RFET device with different dimensions. Tunneling current dominates when the gate voltage exceeds the threshold voltage of the device. Below the threshold voltage, thermionic emission current dominates. Fig. 7 (b) [7] highlights the comparison of the electrical characteristics of SG-RFET device with GAAFET device. The characterization and mathematical analysis of the non-planar device structure –SG-RFET is reported in [16]. The sub-threshold current model and surface potential model of the SG-RFET device derived in [16] show near agreement with the simulation results. The electrical characterization of the SG-RFET and analog and digital circuits implemented using SG-RFET device reported in [7-8] shows good performance in terms of gain, bandwidth and output characteristics. The digital circuits implemented using these multigate devices are presented in [17]. To enhance the current drive of SG-RFET, the mobility of the charge carriers is increased by using strained silicon as channel.

(a) (b)

Fig. 6 (a) SG-RFET (b) GAAFET implemented in TCAD Sentaurus tool



(a) (b)

Fig. 7 (a) I_D- V_G Characteristics of SG-RFET device for different device dimensions
(b) I_D- V_G characteristics of SG-RFET and GAAFET device

The OTA buffer circuits simulated using strained silicon channel SG-RFET device are also discussed in [7,8]. The SG-RFET with gate length (L_G) 50nm and device length (L_T) 220nm and GAAFET with gate length 50nm is chosen for the OTA circuit implementation. The simulation results of two–stage OTA buffer configurations implemented using planar MOSFET and multigate transistors are presented in the next section.

3. RESULTS AND DISCUSSION

3.1. Buffer configuration 1

Buffer configuration 1 with resistive load is implemented using OTA types, namely FC-OTA, RFC-OTA, Simple OTA and Nauta's OTA, and the circuit performance is analysed using different resistive load. For driving a heavy resistance load (< 1 kΩ), a large current is required to attain a better output swing which results in increase in power dissipation. It is observed that increase in g_m can increase the load driving capability that results in high output swing. Moreover, the transconductance of the OTA should be increased to get any significant voltage gain (less than unity), particularly for heavy load, R_L. Table 2 shows the simulation results of buffer configuration 1 implemented using different OTA configurations.

Buffer configuration 1 implemented using SG-RFET OTA and GAAFET OTA are also analysed in Sentaurus TCAD tool. The inverter using SG-RFET device is also presented in [7-8,16] which is compared with the GAAFET inverter. The SG-RFET inverter circuit has a bandwidth of 650 MHz and a gain of 70 V/V. SG-RFET based inverter has a lower propagation delay (20 ps for C_L = 0.35 fF, V_{DD} = 2 V) due to the lower equivalent RC switching delay when compared to the GAAFET device [8].

Table 2 Buffer configuration 1 using CMOS OTAs

Parameters	OTA Type			
	Recycled Folded cascode OTA (RFC-OTA)	Folded Cascode (FC-OTA)	Simple OTA [2]	Nauta's OTA
Technology node (nm)	180	180	180	180
Supply Voltage (V)	±0.9	±0.9	±0.9	±0.9
R_L (kΩ)	5	5	5	5
Gain (V/V)	0.98	0.97	0.96	0.97
UGB (MHz)	48	11	5200	5000
g_m (mS)	7.5	6	5	6

OTA topology using SG-RFET inverter circuit is used in the OTA buffer configurations which is able to drive resistive load < 1 kΩ. Table 3 presents the simulation results obtained for the buffer configuration 1 using multi-gate transistors. Due to the dense meshing at the interface regions in the device, it is difficult to simulate the circuit with more components in Sentaurus TCAD tool. The OTA configuration used in the circuit simulation is Nauta's OTA as it contains only inverter blocks. The circuit parameters used in the TCAD simulation

Table 3 Buffer configuration 1 using multigate transistors

Parameters	OTA Type			
	GAAFET OTA [7]	SG-RFET OTA [7]	Strained Si channel SG-RFET OTA [7]	CMOS Nauta's OTA
Supply Voltage (V)	2	2	2	2
R_L (kΩ)	5	5	5	5
Gain (V/V)	0.98	0.97	0.96	0.97
UGB (GHz)	5.8	0.56	0.78	3.5
g_m (mS)	1	0.79	0.9	0.9

(multigate transistors) are supply voltage V_{DD} = 2 V, output load resistance, R_L = 1 kΩ, input sinusoidal signal amplitude, V_{p-p} = 1 V, and frequency 10 kHz. It is observed that GAAFET OTA based buffer 1 has wide bandwidth and gain closer to unity for a resistive load of 1 kΩ compared to other OTA based buffer configuration 1.

3.2. Buffer configuration 2

Table 4 present the simulation results of two-stage buffer configuration 2 using Simple OTA, FC OTA, RFC OTA and Nauta's OTA respectively. From the simulation results, it is observed that buffer configuration 2 implemented using simple OTA performs better when compared to that using FC OTA, RFC OTA and Nauta's OTA. Two-stage buffer configuration 2 circuit using non-planar transistor OTAs (SG-RFET OTA, strained silicon SG-RFET OTA and GAAFET OTA) are characterized in Sentaurus TCAD tool.

Using device module in TCAD tool, DC and AC analysis of the two-stage buffer 2 are carried out with resistive load. The circuit parameters used in the simulation are supply voltage V_{DD} = 2 V, output load resistance, R_L = 1 kΩ, input sinusoidal signal amplitude, V_{p-p} = 1 V, and frequency 1 kHz. For two-stage buffer 2 using SG-RFET OTA and GAAFET OTA, a peak-to-peak amplitude of 0.99 V is obtained as output from the simulation results, that results in a gain of 0.99 V/V.

Table 4 Two-stage buffer configuration 2 using CMOS OTAs

Parameters	OTA Type			
	Recycled Folded cascode OTA (RFC-OTA)	Folded Cascode (FC-OTA)	Simple OTA [2]	Nauta's OTA
Technology node (nm)	180	180	180	180
Supply Voltage (V)	±0.9	±0.9	±0.9	±0.9
R_L (kΩ)	1	1	1	1
Gain (V/V)	0.99	0.99	0.99	0.99
UGB (MHz)	48	11	5200	5000
g_m (mS)	7.5	6	5	6

As the R_L reduces, the buffer circuit's gain reduces as expected. Table 5 presents the simulation results of buffer 2 configuration implemented using different multigate OTAs. The performance of the SG-RFET OTA buffer amplifier is compared with GAAFET OTA. GAAFET OTA based buffer 2 configuration exhibits a wide bandwidth of 5 GHz for R_L as 1 kΩ

Table 5 Two-stage buffer 2 configuration using multigate transistors

Parameters	OTA Type			
	GAAFET OTA [7]	SG-RFET OTA [7]	Strained Si channel SG-RFET OTA [7]	CMOS Nauta's OTA
Supply Voltage (V)	2	2	2	2
R_L (kΩ)	1	1	1	1
Gain (V/V)	0.99	0.99	0.99	0.99
UGB (GHz)	5.8	0.56	0.78	3.5
g_m (mS)	1	0.79	0.9	0.9

3.3. Single–stage variable gain buffer configuration

N-stage tunable gain CMOS OTA buffer amplifiers named as buffer configuration 3 are presented in [2]. A Monte Carlo simulation has been carried out for two-stage buffer configuration 3 using RFC-OTA, FC-OTA and simple OTA to verify the robustness of the design against process mismatch. Buffer configuration 3 is useful in many applications such as biomedical application, consumer electronics, video applications and other industrial applications.

Figs. 8 (a) - (d), 9 (a) – (d) and 10 (a) - (d) show the distribution of unity gain bandwidth (UGB) and bandwidth of two stage buffer 3 with R_L = 50 Ω, gain variation of buffer 3 with R_L = 50 Ω, gain = 1 V/V and gain variation of buffer 3 with R_L = 50 Ω, gain =5 V/V respectively for 300 samples (N), along with respective mean (μ) and standard deviation (σ) for Simple OTA, FC OTA and RFC OTA respectively. It is observed from the plots that proposed buffer 3 using simple OTA is robust even with local mismatches.

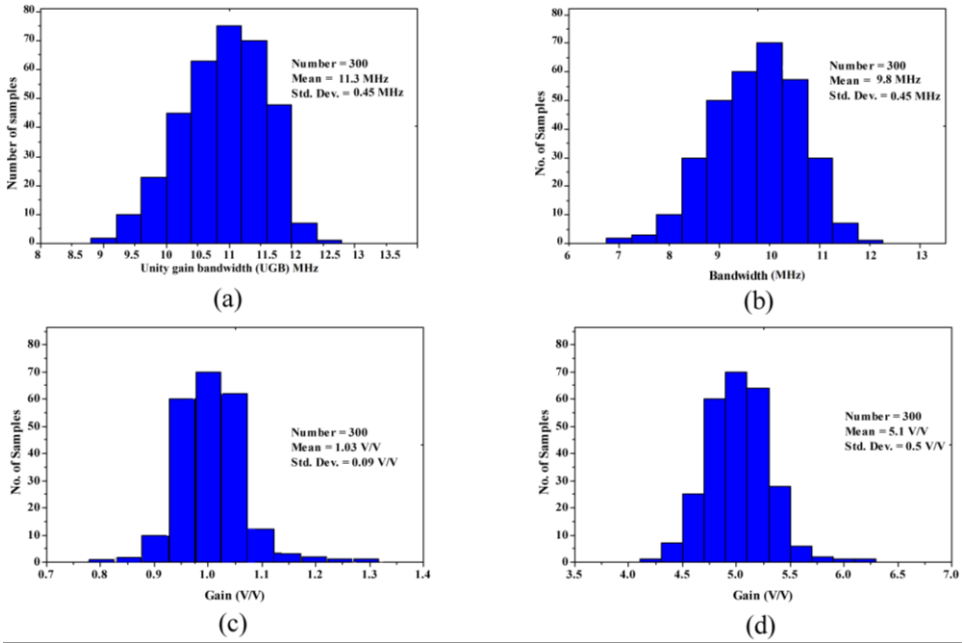


Fig. 8 (a) Distribution of UGB of simple OTA (b) bandwidth of two stage buffer configuration 3 with R_L = 50 Ω, (c) gain variation of buffer 3 with R_L = 50 Ω, gain = 1 V/V and (d) gain variation of buffer 3 with R_L = 50 Ω, gain = 5 V/V respectively for 300 samples (N)

Fig. 8(a) presents the distribution of UGB of simple OTA, Fig. 8 (b) presents bandwidth of two stage buffer configuration 3 with R_L = 50 Ω, Fig. 8 (c) shows gain variation of buffer 3 with R_L = 50 Ω, gain = 1 V/V and Fig. 8((d) shows gain variation of buffer 3 with R_L = 50 Ω, gain = 5 V/V respectively for 300 samples (N).

Fig. 9 (a) presents the distribution of UGB of FC- OTA, Fig. 9 (b) shows bandwidth of two stage buffer configuration 3 with RL = 50 Ω, Fig. 9 (c) shows gain variation of buffer 3 with RL = 50 Ω, gain = 1 V/V and Fig. 9 (d) presents gain variation of buffer 3 with RL = 50 Ω, gain = 5 V/V respectively for 300 samples (N). It is observed from the plots that proposed buffer 3 using simple OTA is robust even with local mismatches. It is observed from the plots that proposed buffer 3 using simple OTA is robust even with local mismatches.

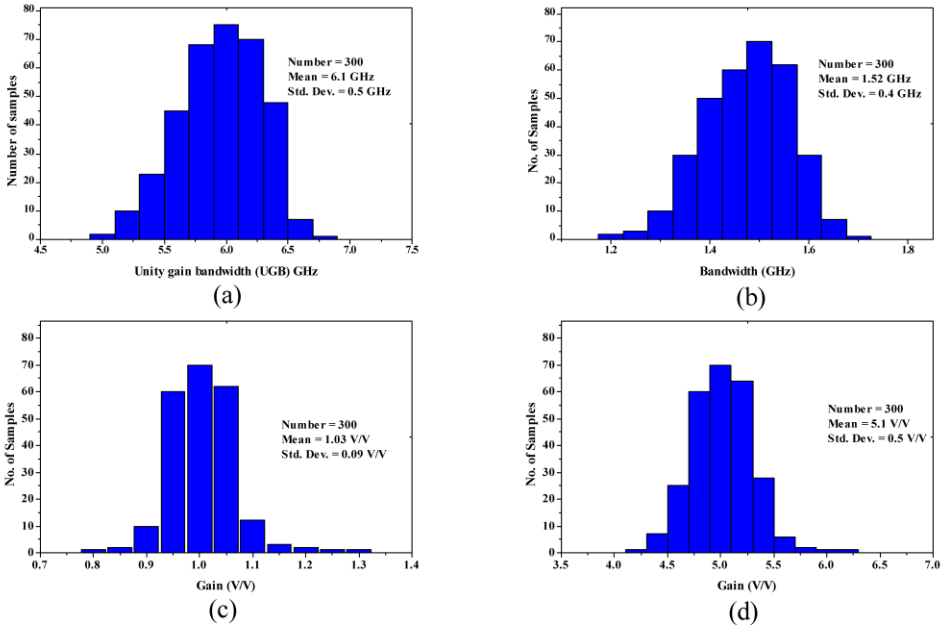


Fig. 9 (a) Distribution of UGB of FC- OTA (b) bandwidth of two stage buffer configuration 3 with R_L = 50 Ω, (c) gain variation of buffer 3 with R_L = 50 Ω, gain = 1 V/V and (d) gain variation of buffer 3 with R_L = 50 Ω, gain = 5 V/V respectively for 300 samples (N)

Fig. 10 (a) presents the distribution of UGB of RFC OTA. Fig. 10(b) presents bandwidth of two stage buffer configuration 3 with RL = 50 Ω, Fig. 10 (c) shows gain variation of buffer 3 with RL = 50 Ω, gain = 1 V/V and Fig. 10 (d) depicts the gain variation of buffer 3 with RL = 50 Ω, gain = 5 V/V respectively for 300 samples (N). For a two-stage buffer configuration 3 requires four OTAs including the feedback circuit. For N = 1, the buffer configuration 3 reduced to a configuration as shown in Fig.11, named buffer configuration 4 which can drive resistive load which is presented in [7]. The feedback factor depends both on the gain and output load of the proposed OTA buffer configuration (buffer configuration 4). In buffer configuration 4, orthogonal gain tuning with load is not possible as in buffer configuration 3.

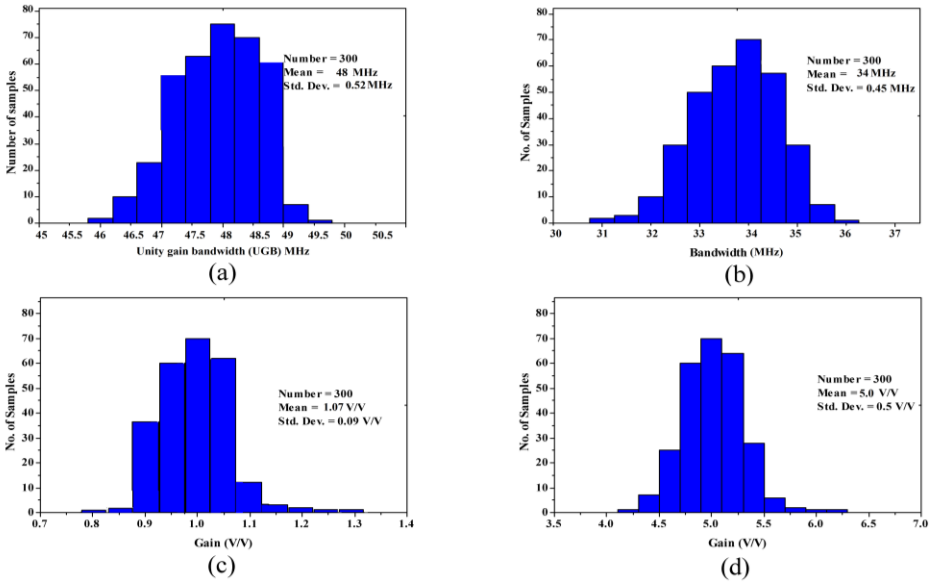


Fig. 10 (a) Distribution of UGB of RFC OTA (b) bandwidth of two stage buffer configuration 3 with R_L = 50 **Ω**, (c) gain variation of buffer 3 with R_L = 50 **Ω**, gain = 1 V/V and (d) gain variation of buffer 3 with R_L = 50 **Ω**, gain = 5 V/V respectively for 300 samples (N)

Table 6 Single –stage variable gain OTA buffer configuration

Parameters	OTA Type			
	Recycled Folded cascode OTA (RFC-OTA)	Folded Cascode (FC-OTA)	Simple OTA	Nauta's OTA
Technology node (nm)	180	180	180	180
Supply Voltage (V)	±0.9	±0.9	±0.9	±0.9
R_L (k**Ω**)	1	1	1	1
Gain (V/V)	1	1	1	1
UGB (MHz)	42	9.3	5000	4800
g_m (mS)	7.5	6	5	6

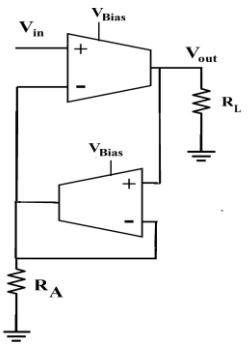


Fig. 11 Buffer configuration 4

As the feedback factor depends on both the gain and output load, the maximum output swing that can be attained for this configuration is limited. Table 6 present the simulation results of buffer configuration 4 using Simple OTA, FC OTA, RFC OTA and Nauta's OTA respectively. Table 7 presents the simulation results of the multigate OTA based buffer configuration 4. It is observed that the GAAFET OTA buffer configuration 4 has a wide-bandwidth as the GAAFET OTA has a UGB of around 5.4 GHz. Simple design, low fabrication complexity, reconfigurable property and reduced area make SG-RFET OTA buffer outperform the GAAFET OTA buffer and CMOS OTA buffer configurations. It is observed that GAAFET OTA buffer has wide bandwidth compared to other multigate OTAs presented in this paper.

Table 7 Single-stage variable gain OTA buffer using multigate transistors

Parameters	OTA Type			
	GAAFET OTA [7]	SG-RFET OTA [7]	Strained Si channel SG-RFET OTA [7]	CMOS Nauta's OTA
Supply Voltage (V)	2	2	2	2
R_L (kΩ)	1	1	1	1
Gain (V/V)	1	1	1	1
UGB (GHz)	5.4	0.38	0.6	3
g_m (mS)	1	0.79	0.9	0.9

3.4. Experimental results

From the simulation results, it is observed that the performance of the OTA buffer amplifier depends on the OTA configuration used in the design. Simple OTA shows better performance in terms of stability when compared with FC-OTA and RFC-OTA. Simple OTA configuration is selected for the hardware implementation of the OTA buffer configurations. The CMOS OTA buffer configurations namely buffer 1, buffer 2 and buffer 3 are fabricated in a single IC at SCL Chandigarh. The die size is 2 mm x 2 mm. The silicon area required for buffer configuration 1, buffer configuration 2 and buffer configuration 3 in the chip area is 54 µm x 45 µm, 250 µm x 85 µm and 235 µm x 160 µm respectively. 32 pin QFN packaging type is used for the buffer IC. The bonding diagram with I/O pads of buffer IC is shown in Fig. 12 (a). The simplicity in this buffer configuration is the feedback fractions can be set externally with respect to the load and gain. Figure 12 (b) shows the experiment set up for testing the buffer IC. The experimental results are discussed in detail in [1].

The layout of the basic OTA used in the buffer configurations for hardware implementation is shown in Fig. 13. The buffer IC contains buffer configuration 1, buffer configuration 2 (three and four stage) and buffer configuration 3 (three and four stage) and also the feedback circuits which is connected to a common supply voltage. The bandwidth of the buffer IC is limited due to the I/O pads used in designing the buffer IC. The simulation results of the buffer IC with I/O pads show that the bandwidth is limited to 150 MHz. Without the I/O pads, the post-layout simulation of each buffer amplifier (buffer configuration 1, buffer configuration 2 and buffer configuration 3) in the IC shows a bandwidth above 900 MHz. The parasitic components in the routing also reduces the bandwidth of the buffer amplifier configuration.

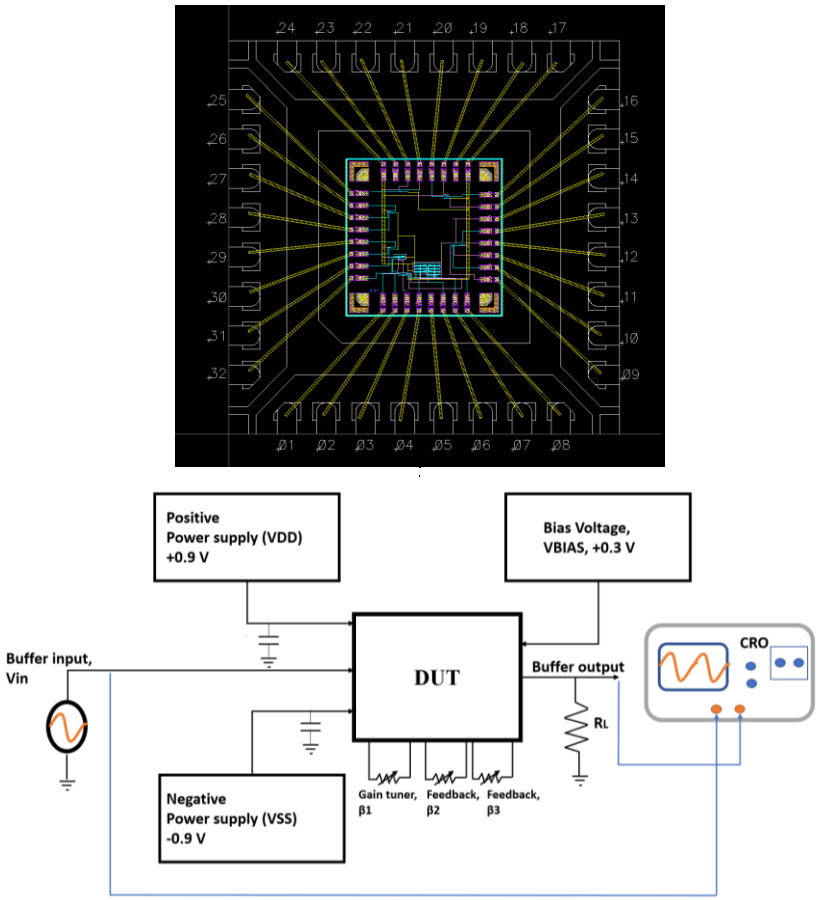


Fig. 12 (a) Bonding diagram of Buffer IC [1] (b) Expeérimental set up [1]

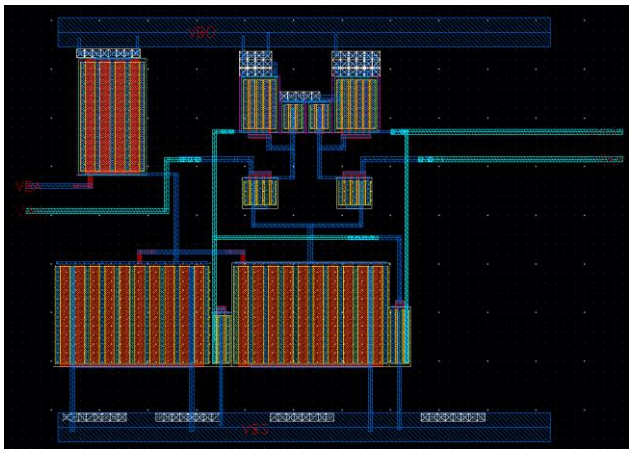


Fig. 13 Layout of the simple OTA

The output obtained from the buffer IC is compared with the simulation results. Figure 14 (a) and (b) highlight the comparison of the gain with respect to load variation of buffer configuration 1 and buffer configuration 2. As the load reduces, the gain reduces due to the loading effect.

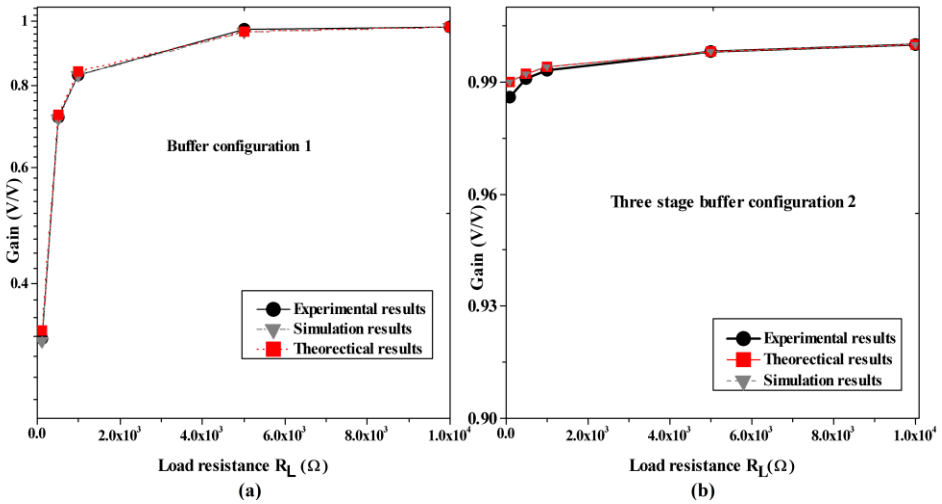


Fig. 14 Comparison of the gain with respect to load variation of (a) buffer configuration 1 and (b) buffer configuration 2 for different load values

As the output impedance is reduced for the buffer configuration 2 due to the voltage series feedback, the gain remains close to unity for an output load upto 100 **Ω**. The gain (A_V) [2] and output impedance (Z_{out}) [2] of the buffer 2 configuration is given as

$$A_v = \frac{1}{1+\left(\frac{g_o}{g_m}\right)^N \left(1+\frac{G_L}{g_o}\right)} \tag{1}$$

$$Z_{out} = \frac{1/g_o}{1+\left(\frac{g_m}{g_o}\right)^N} \tag{2}$$

where g_o and g_m are the output conductance and transconductance of the OTA in the buffer configuration 2, G_L is the output load of the buffer configuration. As N increases, the gain increases (close to unity) for low output load (R_L). The output impedance of the buffer configuration 2 reduces with increase in N. Figure 14 (a) and (b) presents the variation in gain with respect to different output load.

With $V_{out}/V_{in} = \alpha$, gives the value of the feedback factor, β_1 [2] as:

$$\beta_1 = \frac{1}{\alpha} - \frac{g_{o1}}{g_{m1}} \tag{3}$$

where g_{o1} and g_{m1} are the output conductance and transconductance of the first stage OTA in the buffer configuration 3. Using Eq. (3), the feedback factor to obtain the required gain can be determined.

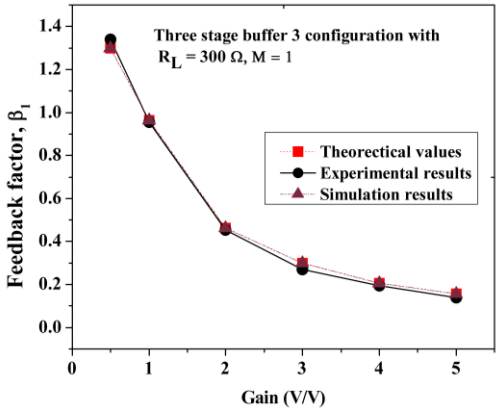


Fig. 15 Gain dependent feedback factor

The main advantage of this configuration is gain tuning is independent of the output load. The mismatch in the experimental results with the theoretical values for low resistance load is due to the assumptions made in the theoretical analysis that OTAs used in the buffer configuration are identical. In actual case there is a slight mismatch in the OTA parameters due to the transistor mismatch or process variations that results in deviation of the experimental results with theoretical and simulation results. As the load reduces, the effect of variation in the parameters of OTA is dominant as the g_m and g_o of each OTA decides the output impedance of buffer configurations.

Figure 15 shows the values of the feedback factor for different gain values calculated using the feedback factor equations derived in [2]. It is observed from Fig. 14 and Fig. 15 that the experimental results show near agreement with the theoretical results and simulation results. Figure 15 depicts the comparison of experimental, simulation and theoretical values of gain dependent feedback factor for different gain which near values. For buffer configuration 3, gain tuning of upto 5 V/V and output swing of 1 V are achieved with R_L equal to 50 Ω. Hence, the OTA buffer configurations are found useful in ADCs, DACs, PLLs, automatic gain control circuits where tunable gain is preferred.

4. CONCLUSION

All-OTA buffer configurations capable of driving resistive load implemented using different CMOS OTA topologies are discussed in this paper. Experimental results of CMOS OTA buffer configurations using simple OTA show near agreement with the theoretical values. CMOS OTA buffer with tunable gain is useful in CMOS ICs for applications such as biomedical application, consumer electronics, video applications and other industrial applications. OTA buffer circuits using GAAFET OTA, SG-RFET OTA and strained silicon SG-RFET OTA with resistive load are analysed in TCAD Sentaurus tool. GAAFET OTA buffer circuit outperform the other multigate OTA buffer circuit in terms of bandwidth. The simulation results show the feasibility of non-planar transistor circuits in analog circuit design. The OTA buffer configurations using multigate transistor OTAs will be useful in applications such as biomedical devices, ADC drivers and wireless sensor nodes.

REFERENCES

[1] R. Jayachandran, K. J. Dhanaraj and P. C. Subramaniam, "Hardware realization and testing of multistage OTA buffer amplifier for heavy resistive load", In Proceedings of 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 550–554.

[2] R. Jayachandran, P. C. Subramaniam and K. J. Dhanaraj, "A novel tunable gain CMOS buffer amplifier for large resistive loads", *Integration*, vol. 77, pp. 1–12, March 2021.

[3] Y. Ha, M. Li and A. Q. Liu, "A new CMOS buffer amplifier design used in low voltage MEMS interface circuits", *Analog Integ. Circuits Signal Process.*, vol. 27, no. 1–2, pp. 7–17, Apr. 2001.

[4] K. Moolpho and J. Ngarmnil, "Low voltage high-performance class-AB FGMOS buffer", in Proceedings of IEEE Asia Pacific Conference on Circuits and Systems, 2006, pp. 1779–1782.

[5] C. Mohan and P. M. Furth, "A 16-Ohm audio amplifier with 93.8-mW peak load power and 1.43-mW quiescent power consumption", *IEEE Trans. Circuits and Systems II: Express Briefs*, vol. 59, no. 3, pp. 133–137, March 2012.

[6] X. Qiu, D. Chen and Z. Wang, "Response of ring oscillator to periodic interference on the power supply", *AEU-Int. J. Electron. Commun.*, vol. 82, pp. 383–390, Dec. 2017.

[7] J. Remya et. al., "High performance reconfigurable FET for a simple variable gain buffer amplifier design", *Int. J. Electron.*, Apr. 2021. (published online)

[8] R. Jayachandran, R. S. Komaragiri and P. C. Subramaniam, "Reconfigurable circuits based on Single Gate Reconfigurable Field-Effect Transistors", In Proceedings of 6th IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), 2020, pp.1–5.

[9] V. Khadem et. al., "An analytical approach to model capacitance and resistance of capped carbon nanotube single electron transistor", *AEU-Int. J. Electron. Commun.*, vol. 90, pp. 97–102, June 2018.

[10] Y.-M. Lin et. al., "High-performance carbon nanotube field-effect transistor with tunable polarities", *IEEE Trans. Nanotechnol.*, vol. 4, no. 5, pp. 481–489, Sept. 2005.

[11] G. Darbandy, M. Claus and M. Schröter, "High-performance reconfigurable Si nanowire field-effect transistor based on simplified device design", *IEEE Trans. Nanotechnol.*, vol. 15, no. 2, pp. 289–294, March 2016.

[12] A. Heinzig et. al., "Reconfigurable Silicon nanowire transistors", *Nano Letters*, vol. 12, no. 1, pp. 119–124, Nov. 2011.

[13] W. M. Weber et. al., "Tuning the polarity of Si-nanowire transistors without the use of doping", in proceedings of 8th IEEE Conference on Nanotechnology, NANO'08, 2008, pp. 580–581.

[14] F. Wessely, T. Krauss and U. Schwalke, "CMOS without doping: Multi-gate silicon-nanowire field-effect-transistors", *IEEE J. Solid-State Circ.*, vol. 70, pp. 33–38, Apr. 2012.

[15] D. Sacchetto, Y. Leblebici and G. De Micheli, "Ambipolar gate-controllable SiNW FETs for configurable logic circuits with improved expressive capability", *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 143–145, Feb. 2012.

[16] R. Ranjith et. al., "Two dimensional analytical model for a reconfigurable field effect transistor", *Superlattice. Microstruct.*, vol. 114, pp. 62–74, Feb. 2018.

[17] R. S. Assaad and J. Silva-Martinez, "The recycling folded cascode: A general enhancement of the folded cascode amplifier", *IEEE J. of Solid-State Circ.*, vol. 44, no. 9, pp. 2535–2542, Sept. 2009.

[18] A. S. Khade, V. Vyas and M. Sutaone, "Performance enhancement of advanced recycling folded cascode operational transconductance amplifier using an unbalanced biased input stage", *Integration*, vol. 69, pp. 242–250, Nov. 2019.

[19] D. Binkley, B. Blalock and J. Rochelle, "Optimizing drain current, inversion level, and channel length in analog CMOS design", *Analog Integ. Circuits Signal Process*, vol. 47, no. 2, pp. 137–163, March 2006.