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Original scientific paper

ACTIVE INDUCTOR BASED LOW PHASE NOISE VOLTAGE CONTROLLED OSCILLATOR

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Abstract. *This paper proposed a fully MOS-based voltage-controlled oscillator (VCO) with tuning range and low phase noise, replacing the most often used NMOS-based inductor-capacitor tank arranged in cross-coupled topology with a high-Q active inductor. This study mainly focuses on VCO design using a MOS-based active inductor and is implemented and verified using UMC 180nm CMOS technology. The proposed VCO is resistorless and consists of an active inductor, two MOS capacitors, and the buffer circuits. The fundamental principle of this MOS-based VCO concept is to use MOS based inductor to replace the passive inductor, which is an active inductor that gives less area and low power usage. At 1 MHz frequency offset, the phase noise achieved by this proposed configuration is -102.78dBc/Hz. In the proposed VCO architecture, the frequency tuning range is 0.5GHz to 1.7GHz. This VCO design can accomplish this acceptable tuning range by altering the regulating voltage from 0.7V to 1.8V. This suggested architecture of proposed VCO design has the power consumption of 9mW with a 1.8V supply voltage. The suggested VCO has been shown to be a good fit for low-power RF circuit applications while preserving acceptable performance metrics.*

Key words: *active inductor, VCO, frequency tuning range, phase noise, power consumption*

1. INTRODUCTION

In several domains such as healthcare fields, military, telecommunications, radar equipment, etc., wireless transceivers have been commonly used [1]. In the exponential growth of transmission technologies such as wireless and diverse uses, integrated circuits based on CMOS technology play a very significant role. The VCO has its benefits in analog signal applications [2]. Low power, high speed, and minimal space are the factors for selecting the CMOS technology. The LC-VCO with a wide range of frequency tuning is the most critical RF building block in the adopted and modern communication system. In wireless communication arrangements, voltage-controlled oscillators provide critical

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performance [3-5]. The depletion of phase noise is managed by attempts at different levels: technology, construction, and overall visualization [5].

We want inductive characteristics for high-speed applications. In making large-speed transceivers, the high efficiency of the inductor plays an essential part. It relies on several specifications and relevant parameters. A ring oscillator can be used as a VCO, an oscillator that supports an LC component or a MOS-based VCO. With positive feedback, the ring oscillator is helpful for large frequency tuning range, but the disadvantage is minor phase noise performance; hence they are not valuable for different communication fields [2,6].

The topology of gyrator-C is easy and convenient in achieving the MOS-based inductor configuration. Two back-to-back transconductors, one of which is connected to a capacitor, make up the primary active inductor [7]. A high-quality (Q) feature is present in the above structure of the active inductor [2]. In comparison to a passive inductor, using an active inductor throughout a VCO increases noise in the entire circuit. When compared to a passive inductor, this active inductance created greater phase noise. The composite trans-conductor VCO is employed to make the most out of this devastating challenge because it exhibits severe phase noise, low power consumption, and chip area reduction. For convenience, the present bias is considered to be independent of VDD [8]. To boost the output amplitude of the oscillation, an external buffer circuit is involved on both sides of the VCO output node.

A new circuit architecture for a VCO using an active inductor is suggested in this study. A unique active inductor is presented in this work to enhance the overall parameter of the LC VCO, such as tunning range, power consumption, and phase noise, at the same time. The recommended research's primary focus is on making the active inductor adjustable by varying the inductor's inductance parameters without causing any physical changes, which is not feasible with spiral inductors [8]—also, making MOS varactor capacitance adjustable by varying the control voltage.

There are separate sections in this proposed paper of VCO. The entire system architecture is discussed in Section II, meaning the function of the inductor topology and the design of the VCO and the principle, and section III show the circuit design based on the active inductor. Section IV describes the simulation results of the proposed VCO using the Cadence environment.

2. Architecture for Active Inductor

2.1 Gyrator Topology

Gyrator-C topology is employed in the creation of an active inductor. The functional topology of the Gyrator-C based Inductor is shown in Figure 1. Forwarding and feedback trans-conductors are the main fundamentals for the structure of an active inductor. If the gyrator port is attached to a capacitor, the whole circuit is called the gyrator-C topology. The entire network acts inductively by connecting a capacitor to the circuit. It provides an inverse relationship between the trans-conductor and the transconductance, respectively [2,9,10,11]. The Gyrator may be used as a dual-mode system. The same source has a trans-conductance that is negative. The great benefit of using a unique topology is that it helps eradicate circuit noise and typical mode interference and creates and attracts them

well. Similarly, it means that the current is out of the trans-conductor while the voltage is positive. By using the feedback loop, the simple inductance equations are as follows:

$$I_{in} = G_{m1} \times V_{in} \tag{1}$$

$$V_{out} = \frac{G_{m1} V_{in}}{SC} \tag{2}$$

$$Z_{in} \cong C_S \times G_{M1} G_{M2} \tag{3}$$

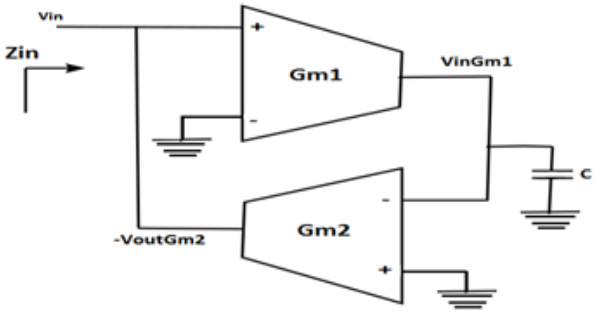

Fig. 1 Gyrator-C topology

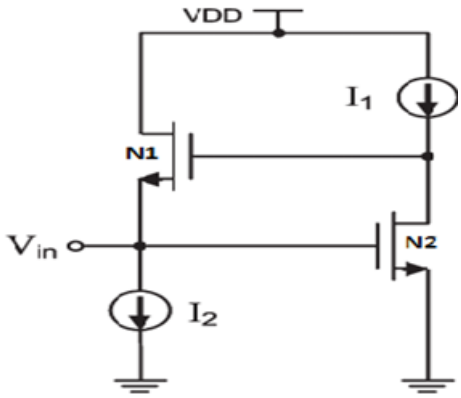

Fig. 2 Single-ended type Active Inductor

The gyrator converts total capacitance into inductance at input terminal Vin. Figure 2 shows the most often used inductor [1], which is composed of two transistors designed to act as an inverting impedances network [12,13]. The transistor threshold voltage is supposed to be Vt, and Vsat is the saturation voltage, so voltage variations on the input side are regulated by Vdd-Vsat-Vod-Vt and Vt+Vod middle, where Vod is the transistor overdrive voltage.

This characteristic is used to calculate the theoretical low power consumption of the active inductor-based voltage-controlled oscillator. Still, on the other hand, as an electric current travels in the non-inductor part of the circuit with limited range, may have been accurately calculated the oscillator's RF output power.

Cascode topology is used to increase the consistency factor and, as expected, to minimize the overall series resistance, a lack of voltage swings can impair the energy flow. That's why we need to move toward a differential active inductor topology. It has two significant benefits over similar circuits [13]:

1) The circuit can avoid common-mode interference and minimize the identical harmonics, much like any other distinct topology;

2) The voltage swing of the differential active inductor is twice as high as the active inductor of the single-ended form.

Figures 3 and 4 show a differential active inductor and an equivalent active inductor circuit, respectively [13].

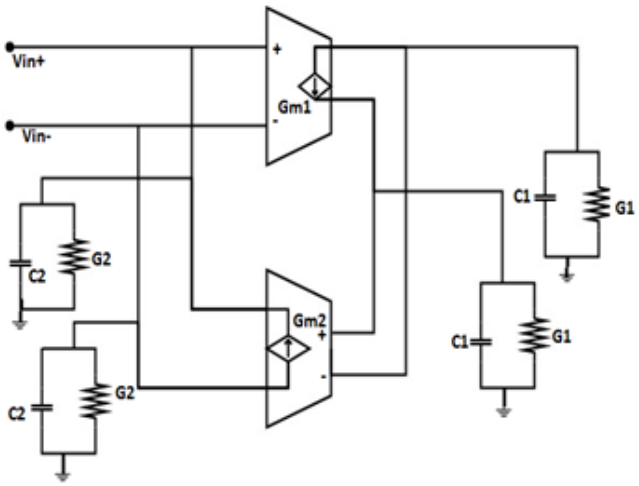

Fig. 3 Differential active inductor

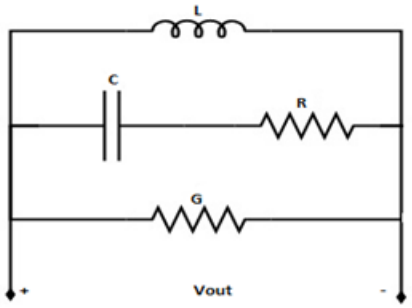

Fig. 4 Equivalent circuit for active inductor

3. VCO CIRCUIT DESIGN

3.1 Conventional LC-VCO

In Figure-5, the primary circuit of the traditional VCO is shown. In cross-coupled pairs, NMOS transistors are used [1]. The LC tank and the formation of negative resistance of the oscillation initial conditions, which are commonly utilised by the cross-coupled pair, are used to measure frequency oscillations [1,14-19]. Only the passive inductor portion will replace the 75-80 percent region of the entire VCO chip, given the supporting passive LC-VCO.

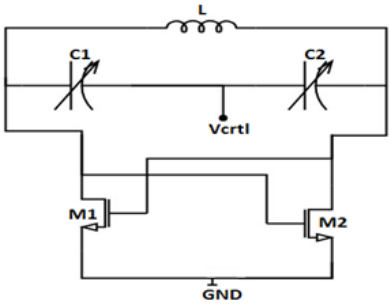

Fig. 5 Conventional LC-VCO

The gyrator-C topology will be used for the creation of an active inductor in this suggested circuit design. The formula below may be used to calculate absolute inductance in the gyrator-C structure:

$$L = \frac{C}{G_{m1}G_{m2}} \tag{4}$$

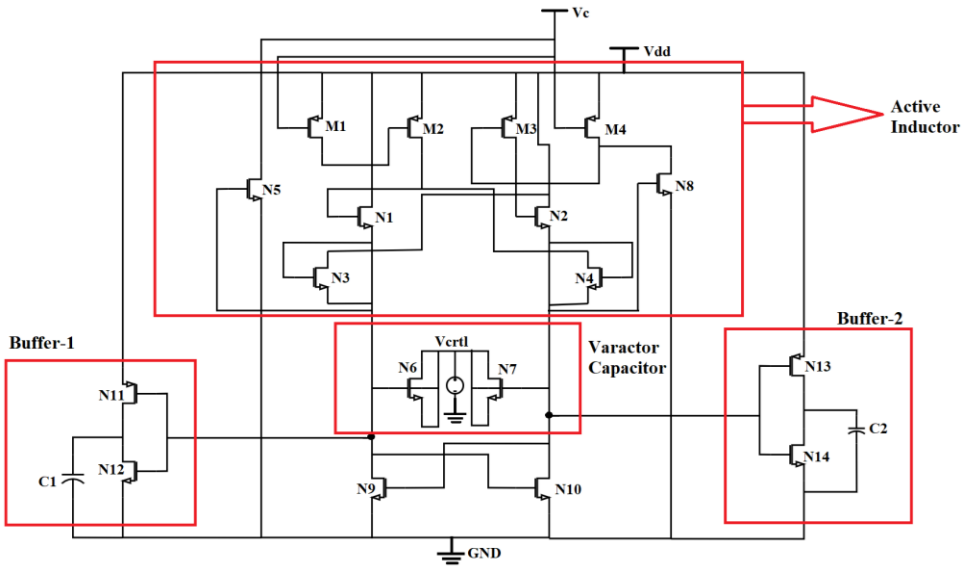

Fig. 6 VCO design using active inductor

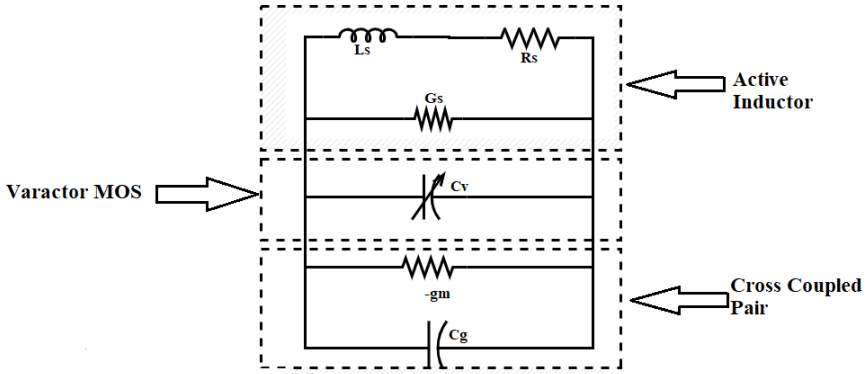

Fig. 7 Equivalent circuit representation of proposed VCO

The equivalent equations are shown below [1]

$$G_s \cong \frac{G_{m7,8}}{2}\left[1 - \frac{G_{m1,8} * G_{gs3,4}}{C_{gs1,8} * G_{m3,4}}\right] \tag{5}$$

$$L_s = \frac{2C_{gs1,2}}{G_{m1,2}G_{m5,8}} \tag{6}$$

$$C_g \cong \frac{1}{2}\left[C_{gs5,8} - \frac{G_{m1,8} * G_{gs3,4}}{G_{m3,4}}\right] \tag{7}$$

Proposed active inductor based VCO design is fully MOS based structure. The LC tank circuit is loaded at the drain terminal, and the differential arrangement is formed by a pair of LC tanks [7]. These NMOSs, which give 180^0 phase shift as they are in typical source configuration, also present another criterion relating the overall phase shift, which is that it should be 0^0 or 360^0 [7]. The capacitor is often replaced by a variable capacitor based on MOS. A schematic diagram of the proposed VCO architecture using an inductor based on MOS is shown in Figure-6, and its equivalent circuit representation is shown in Figure 7 [20]. A MOS-dependent inductor substitutes the passive inductor in a typical LC-VCO, and then the passive capacitor is also replaced by a supplied MOS-based capacitor that is a MOS varactor. Here, additional buffer circuits are attached to increase the amplitude of oscillation. N1 and N2 MOS transistors are used as voltage buffers in Figure-6 and are both related in the configuration of the common mode. The equivalent circuit of the proposed VCO is shown in Figure 7.

As a capacitor with voltage control, MOS varactor are employed. When the drain, source, and bulk of MOS varactor are linked, they behave as a device like a capacitor having C capacitance [20]. The values of the various components utilized to construct a MOS-based VCO are shown in Table 1.

Table 1 Circuit Parameters of the designed VCO

Components	Device Size/ Values
M1, M2, M3, M4	50µm/0.18µm
N1, N2, N9, N10, N11, N12	100µm/0.18µm
N3, N4, N5	50µm/0.18µm
N6, N7, N13, N14	25µm/0.18µm
C1, C2	0.1×10^{-15} F

For reuse, two blocks of Gm are related backward. M2 and M3 MOS serve as existing sources of MOS transistors to limit the inductor inductance quantity. The voltage Vc should be adjusted to the minimum point to get the lowest inductance at the maximum frequency. Transistors N3-N4 should also be biased at the maximum overdrive voltage to produce significant transconductance with the smallest gate capacitors (VGS-VT). We need to give start up condition every time for getting sustained oscillation. For low phase noise of VCO in oscillation, N5 and N8 are used in the active inductor, and transistors M1 and M4 minimize the differences in the same signal. N9 and N10 transistors are used to provide a negative resistance for oscillations. The inductance property is controlled by an external voltage source Vc for the circuit presented. The LC tank comprises the inductor having its parasitic capacitance and the MOS varactor, which is utilized to change the oscillation of frequency. This supply voltage helps direct control of the value of active inductor inductance. With the M1 and M4 MOS transistors, this can be done. On M1 and M4 MOS transistors, we need to increase the control voltage to compensate the low gate voltage. There is another Vcrtl voltage to control the capacitance value fluctuation, which provides more significant phase noise and a higher frequency range compared to others.

The capacitors C1 and C2 behave like DC blockers [2]. These capacitors are used to block the actual circuit and the carrier circuit from interfering. It blocks the circuit's DC signals, thus allowing the high radio frequency signal to pass through.

The design of the above VCO begins with the most straightforward strategy for creating the active inductor, the gyrator-C topology. Using a MOS-based inductor, the voltage-controlled oscillator is built such that the whole system becomes an entirely MOS-based VCO.

4. Post-Layout Simulation Results

The fully integrated MOS-based VCO circuit uses an active inductor built into the UMC 180nm CMOS technology in the Cadence Virtuoso tool. Analysis and simulation were performed using the Cadence software. To achieve sinusoidal oscillation, different characteristics of the suggested design like periodic steady-state (PSS), phase noise analysis, and transient response must be assessed.

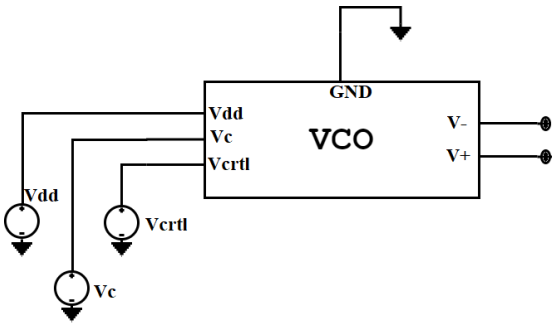

Fig. 8 Block Diagram Representation of proposed VCO

Figure 8 represents the block level representation of the proposed VCO design for post-layout simulation. Figure. 9 shows the layout design of the proposed VCO using an active inductor. The parasitics have a significant impact on the VCO's performance. For

the detection of inductance, parasitic resistance, and parasitic capacitance, RLC extraction (AV extraction) with coupled mechanism has been used. This proposed arrangement has 1293 pcapacitance, 450 resistance, and 357 pinductors in its circuitry inventory. The following parts go through the post-layout extracted and simulated active inductor-oriented VCO. The performance characteristics as a function of tuning voltage, ranging from 0.2 to 2.0 V, are presented in Table 2.

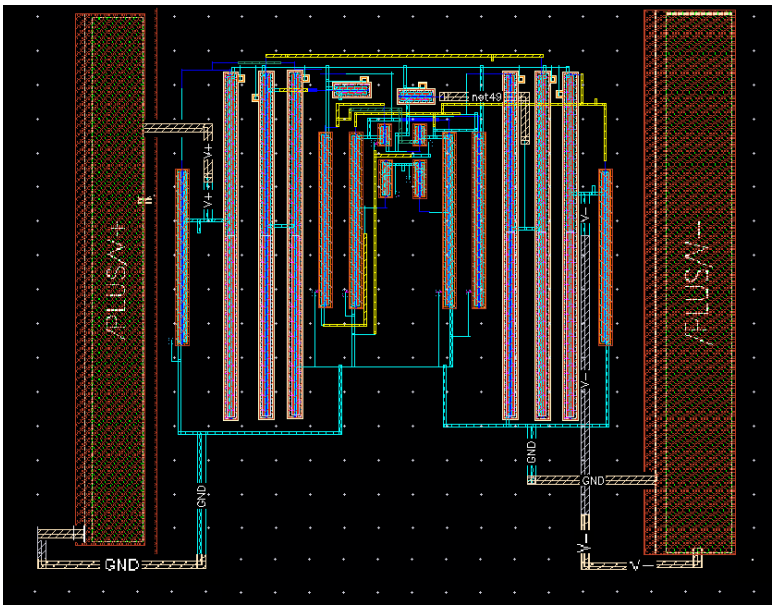

Fig. 9 Layout design of VCO using active inductor

Table 2 Performance summary and comparison of proposed VCO Design

Source	[26]	[10]	[11]	[4]	[18]	[15]	[25]	This Work
Technology	0.18µm CMOS	0.13µm CMOS	0.18µm CMOS	0.18µm CMOS	TSMC 0.18µm	0.35µm	0.18µm CMOS	0.18µm CMOS
Technique	Active inductor	Active inductor	Active inductor	Active inductor	Active inductor	Active inductor	Active inductor	Active Inductor
Frequency Tuning Range	0.55GHz - 3.8GHz	1.22GHz– 2.6GHz	0.5GHz– 2GHz	1.3GHz– 3.8GHz	0.5GHz- 2GHz	680MHz- 1.450GHz	5.5GHz	0.5GHz- 1.7GHz
Phase noise (dBc/Hz)	-89 to -78	- 82 to -87	-78 to -90	-81 to -94	-90.33	-87	-80.314 at 1MHz offset frequency	-102.78 at 1MHz offset frequency
Figure of Merit (FOM)	-133.5 ~ -138.84	-151	-	-	-	-	-140.43	-168.54
Voltage Supply (V)	1.8	1.1	1.8	1.8	-	3.3	1.8	1.8
Power Consumption	11.9mW	3.6mW- 4.3mW	-	-	13.8mW	10.5mW	29.38mW	9mW

The simulated time-domain Output Oscillation vs time plot waveforms derived by transient analysis is shown in Figures 10 (a & b). This VCO has a concise start-up time of 1-2 ns at 1.0 V supply voltage to achieve a steady state. This is a quick technique to check the VCO's operation and determine its settling time and output frequency.

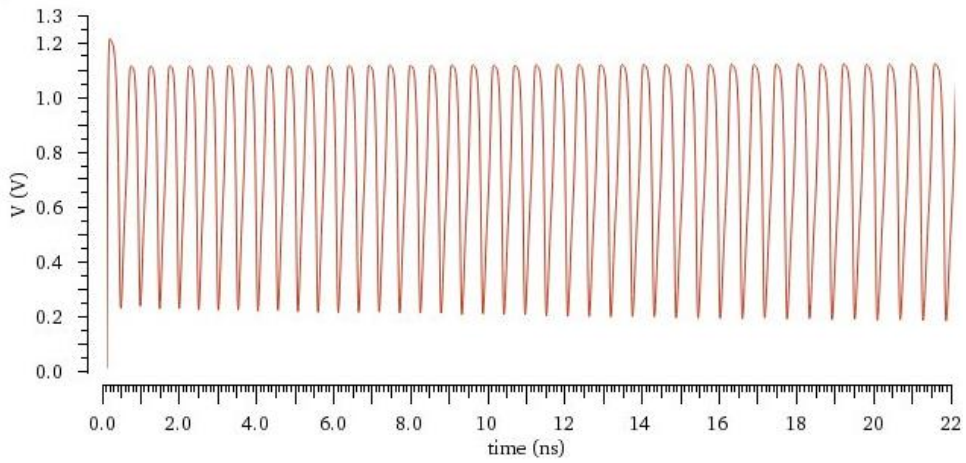

Fig. 10 (a) Single-ended output waveform

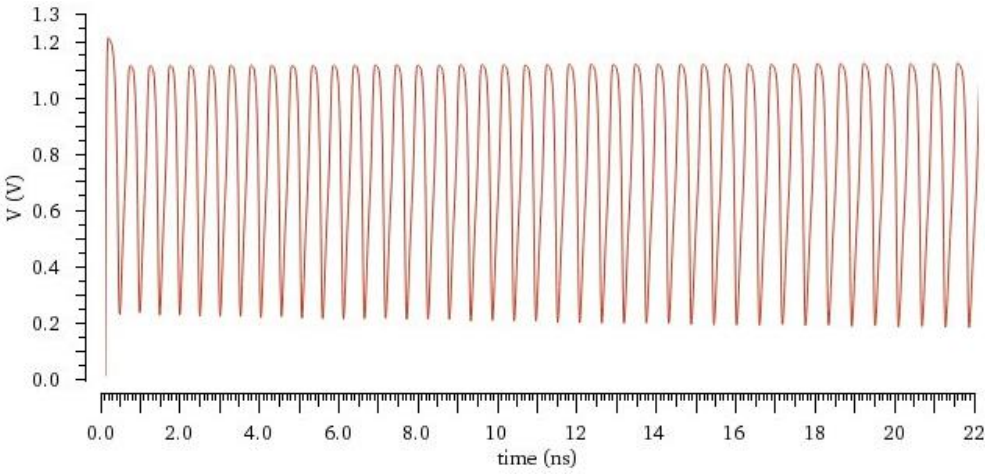

Fig. 10 (b) Differential output waveform

Figure 11 and 12 represent the Periodic steady-state (PSS) analysis plot and phase noise plot for the proposed VCO Design after the post layout simulation. It is evident from the findings below that the VCO has a broad frequency spectrum from 512MHz to 1.7GHz. By changing the voltage Vc from 0.7 to 1.7V, this tunning range can be obtained from equation 8.

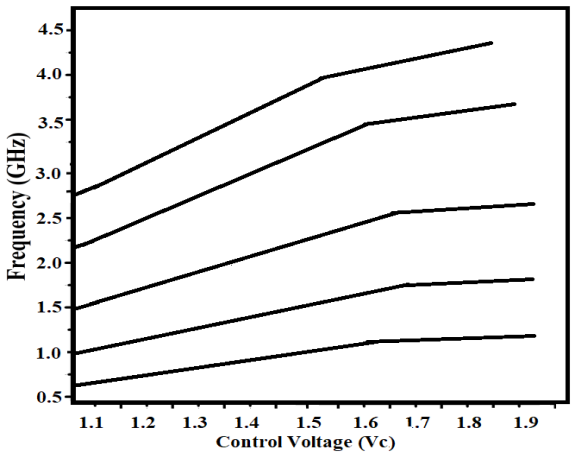

Fig. 11 Periodic steady-state analysis of proposed VCO design

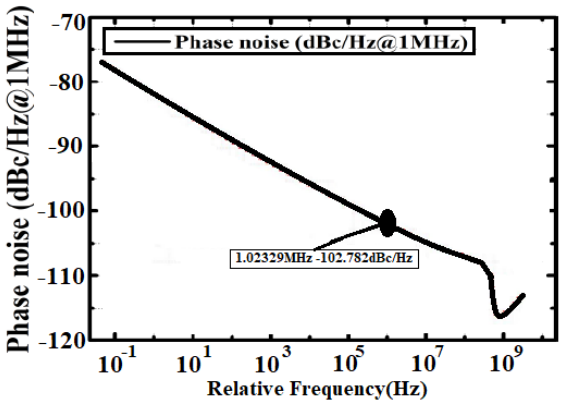

Fig. 12 Phase noise vs Relative Frequency

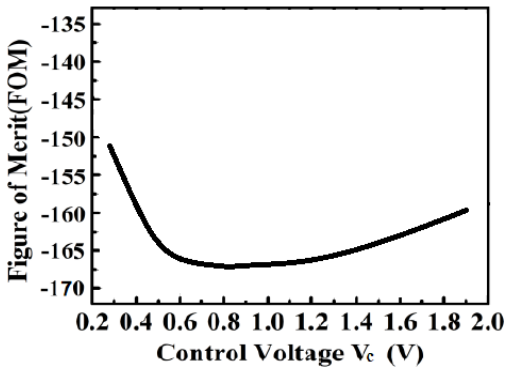

Fig. 13 Figure of Merit vs control voltage

The formula for percentage tunning range can be

$$\% \text{ Tuning range} = \left\{\frac{F_{maximum} - F_{minimum}}{F_c}\right\} \times 100 \quad (8)$$

In Figure 12 phase noise plot for the proposed design is depicted. Here Fc denotes the average frequency, and Fmaximum and Fminimum are the max. and min. Range of frequency concerning 1st harmonic. The phase noise achieved by this VCO configuration is -102.78dBc/Hz at a 1 MHz frequency offset.

Theoretically, Phase noise is also calculated by using Leeson's formula, given in equation 9.

$$L(F_m) = \frac{KT}{2P_c}\left[1 + \frac{F_c}{F_m} + \left(\frac{F_o}{2f_m Q}\right)^2\left(\frac{f_m + f_c}{f_m}\right)\right] \quad (9)$$

The Figure of merit (FOM) of the proposed MOS based VCO has been calculated. The FOM values can be obtained from Eq. (10) [17,21].

$$FOM = L\{f\} + \log\left(\frac{P_{dc}}{1mW}\right) - 20\log\left(\frac{f_o}{F_{offset}}\right) \quad (10)$$

where f_0 is the oscillation frequency. Pdc in the above equation is the power consumption in mW, and L{f} is the phase noise calculated at a frequency offset {f} from the carrier at f_0 [17, 21]. The FOM results of proposed VCO design are shown in Figure-13. It is evident from Eq. 10) that for a certain frequency, the oscillator's FOM is completely dependent on the phase noise and the oscillator's power consumption value. As demonstrated in Table 2, better phase noise at reduced power consumption leads in better FOM of the oscillator.

5. Stability, Temperature Effect & Monte-Carlo Analysis of Proposed VCO Design

Slight changes in process factors like doping levels, oxide thickness of the MOS, junction depths, and so on can impact overall circuit performance. Analog circuits are vulnerable to temperature change when the voltage level is decreased. Thus, a temperature sweep study was performed for various distinct temperatures ranging from -50°C to 50°C. Figures-14 and 15 demonstrate the influence of temperature on the frequency tuning range and phase noise of the VCO, respectively.

Monte Carlo simulations have been performed on the suggested active inductor based VCO design. The Monte Carlo analysis can be used to analyse a circuit's process variance and interface mismatch and its influence on the system. Monte Carlo simulations have been verified with Spectre-RF simulator of Cadence Environment. The Monte Carlo analysis with a 300 sample size was conducted using Gaussian distribution with sigma variations, and the results are depicted in Figure- 16 and 17. For various intervals of the oscillation frequency fvco, they are represented as a frequency of occurrence histogram. To obtain probability statistics, histograms are matched with the Gaussian function. In the condition of Vctrl = 1.2, the oscillation frequency is the necessary range in 95 percent of the occurrences, with a mean value of 1.42 GHz and a σ of 0.018 in Figure. 17.

Figure-16 shows the average power dissipation of the overall proposed circuit. Figure-17 represents the frequency tuning range of the proposed VCO design.

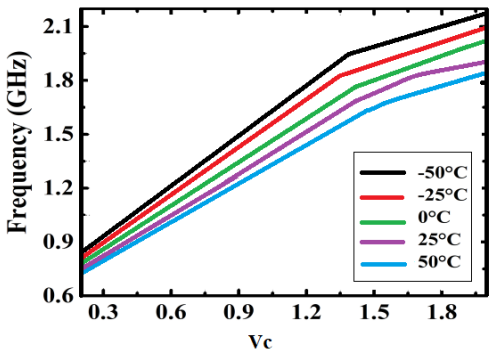

Fig. 14 Temperature effect on VCO frequency tuning range

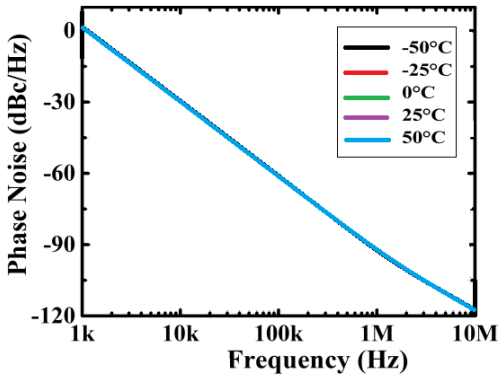

Fig. 15 Temperature effect on VCO phase noise

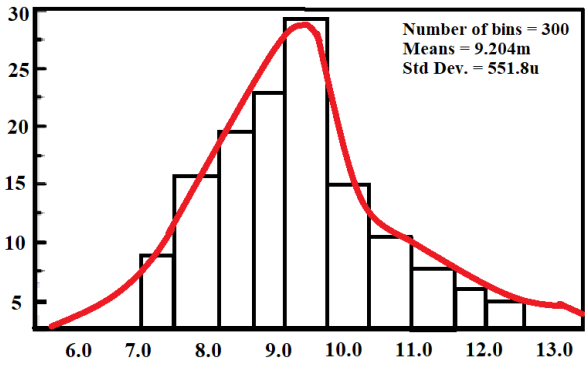

Fig. 16 Average power dissipation (mW)

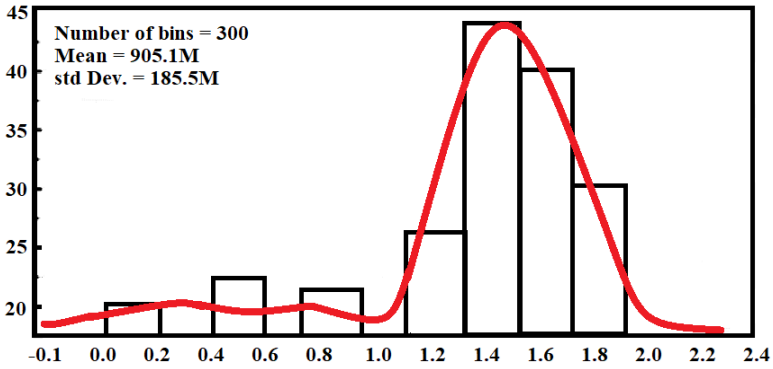

Fig. 17 Frequency tuning range plot (GHz)

6. CONCLUSION

The active inductor topology used in this paper to enhances the frequency of oscillation and reduce the phase noise in the novel MOS-based VCO design is proposed in this work. An active inductor based VCO has been simulated using UMC 180nm technology with the help of a Cadence virtuoso tool. Two NMOS transistors are connected in cross-coupled mode topology. This integrated MOS transistor pairs connected with high-Q active inductor have provided low noise contribution. Such kind of configurations play important role in noise reduction in the circuit. VCO nominal range is 512MHz to 1.7GHz. The Vc variance of the VCO achieves this from 0.7 to 1.7V. For this purpose, we used the standard topology, so the phase noise of the VCO is reduced to -102.78dBc/Hz. These results indicate that the proposed method is feasible and valuable for designing the next-generation chip-transceivers system in conventional silicon technology, perhaps up to the millimetre-wave frequency.

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