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PLUG-AND-PLAY TRANSCEIVER WITH HIGH GAIN AND ULTRA LOW NOISE FIGURE FOR IEEE 802.15.4 APPLICATION

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Abstract. *This paper shows the design and performance simulation of a 2.4 GHz plug-and-play transceiver based on a high speed switch for IEEE 802.15.4 applications. The electrical design was optimized taking into account the scattering parameters, input-output impedance matching and minimum trace width. The simulation results show an important performance regarding the Noise Figure (0.38 dB) and gain (21 dB) at particular temperature for reception mode, transmission scattering parameters (S_{12} and S_{21}) and reflection scattering parameters (all the rest parameters) for both mode operation (Power Amplifier and Low Noise Amplifier).*

Key words: *Power amplifier, low noise amplifier, scattering parameters.*

1. INTRODUCTION

Nowadays, wireless communication systems are necessary to improve and expand the variety of services for the private, public and personal sectors [1,2]. In particular, the concepts of Internet of Things (IoT) and machine-to-machine (M2M) impose a tendency towards the monitoring, control and data acquisition for different types of clients [3]. Although there is a large number of wireless communication systems, these require improvements to some parameters, such as the extension of coverage (i.e. link distance) considering the trade-offs between energy consumption, the complexity of the electronic design, and the cost-effect. In order to improve these parameters, the Power Amplifier (PA) and the Low Noise Amplifier (LNA) are suitable technical options for full-duplex high-end telecomm systems; both have important features such a noise figure, gain, linearity, single / multiple narrow/wide bands and impedance matching [4,5]. However, designing and manufacturing these circuits with high performance for all parameters is a difficult task. Resizing PA and LNA is a trend but the gain-size trade-off is a highlight issue [6,7]. A LNA+PA circuit with higher gain and lower Noise Figure (NF) is required

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for wide coverage applications where plug-in-play transceiver systems are needed [8,9]. In terms of low data rate wireless personal area network technologies, IEEE 802.15.4 is the most useful standard used due to the extended life of the device based on low power consumption [10,11]. Wide coverage applications based on this protocol are a crucial issue that the presented novel and optimum transceiver can solve. We propose a reduced plug-and-play transceiver in comparison with the traditional transceiver. The principal objective of our proposal is to increase the distance of communication links without the digital processing performed in traditional transceiver. This paper is organized as follows: Section 2 is dedicated to the general description of the electrical design. Section 3 shows the simulation results regarding scattering parameters in both operation modes, noise figure and gain performance. Section 4 concludes the paper and mentions the future work for the manufacture of the electrical board with industrial quality level.

2. Electronic Design

Fig. 1 shows the block diagram of the transceiver (PA+LNA), and *MultiSim* software was used for simulation analysis. The general set-up presents the LNA subsystem where the incoming signal is received by the antenna (SMA connector) and fed to a high speed RF switch. The switch presents a high isolation based on a RLC circuit and two diode circuits, i.e. dual switching diode circuit (BAW56LT1) and a high shunt signal isolator / low shunt insertion loss diode (BAR81W) with a switching rate up to 2 GHz. In particular, the RF switch has a control port to commute between transmission and receiver mode. After the LNA block, the electrical signal is fed to another RF switch to send the signal to the processing board. As for the signal path and the way of processing for the PA, it is the same as that of LNA. In addition, two test points were established in order to measure the scattering parameters (*S*-parameters) [12] using a Network Analyzer (NA) for different time slots (i.e., slot #1 for reception mode that relates port #2 as input and port #1 as output, while slot #2 for transmission mode that relates port #1 as input and port #2 as output).

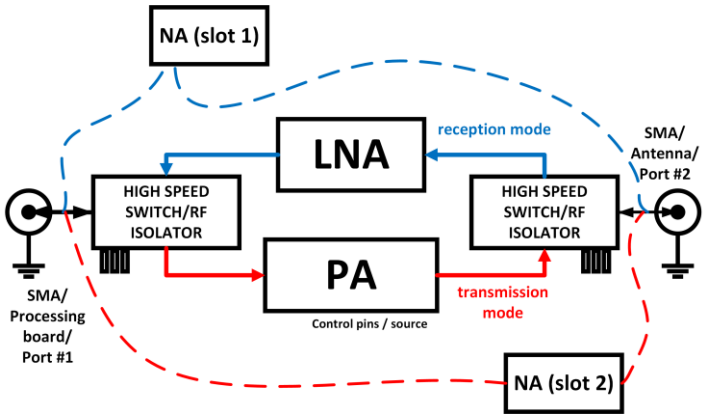

Fig. 1 Block diagram of transceiver. Blue trace describes the LNA-PA path and red trace describes the PA-LNA path with the respective measurement points at slot 1 and 2.

Fig. 2a) shows the general electronic diagram for the high speed switch / RF isolator based on the diodes mentioned for transmission mode. A mode controller is used in order to switch modes using the connection points, *c* and *d*. In particular, the connection point *c*, enables or disables the PA circuit shown in Fig. 2b, and connection point *d* controls the LNA circuit shown in Fig. 3b). While the connection points *a* and *b* are the input and output of the PA circuit. An Input-Matching-Impedance-Network (IMN) and Output-Matching-Impedance-Network (OMN) were implemented in the input and output port of the PA, respectively, as Fig. 2 shows.

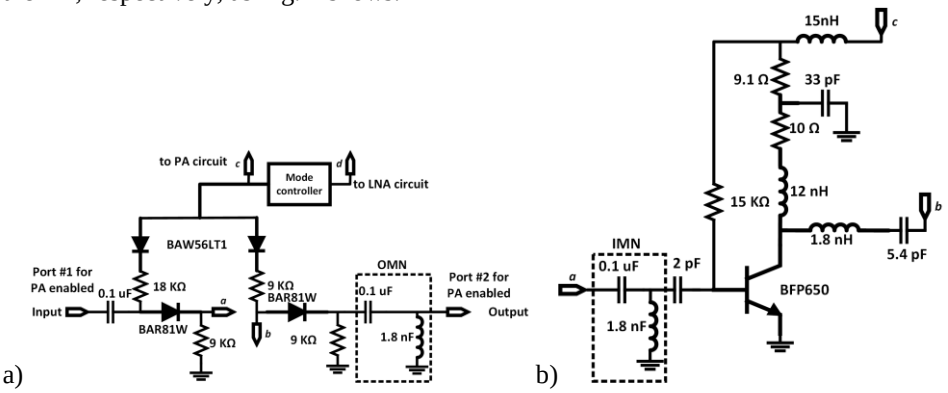

Fig. 2 a) Electronic diagram for high speed switch / RF isolator for transmission mode, b) Electronic diagram of the PA.

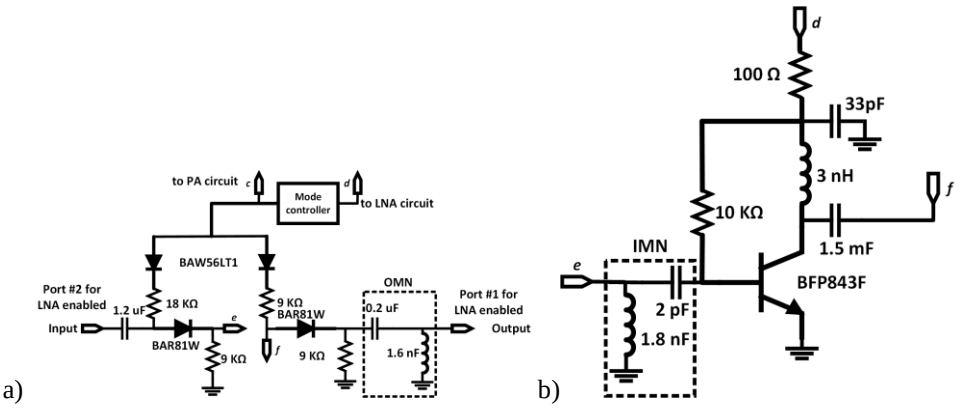

Fig. 3 a) Electronic diagram for high speed switch / RF isolator for reception mode, b) Electronic diagram of LNA.

Fig. 3a) shows the general electronic diagram for the high speed switch / RF isolator for reception mode. In general, the electronic diagrams shown in Fig. 2a) and 3a) are similar, however, particular inductance and capacitance values are modified in order to optimize the IMN and OMN. In addition, the connection points, *e* and *f*, represent the input and output of the LNA circuit. As mentioned, the PA circuit uses the BFP650 transistor, therefore, the first step of the design is to measure the current-voltage

characteristics in order to choose and set the *Q*-point (operating or quiescent point). Fig. 4 shows the relation between the V_{CE} and I_C for different I_b, where the trace corresponding to I_b = 6 mA was selected for V_{CE} = 3.3 V in order to establish proper operating conditions (*Q*-point) based on the input data signal. The same procedure was performed to determine the *Q*-point of the BFP843F used in the LNA circuit and the same biasing voltage (V_{CE}) was chosen.

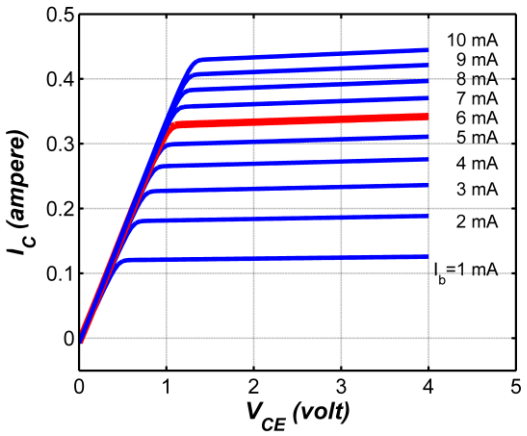

Fig. 4 Analysis of the transistor BFP650. Blue trace describes the V_{CE}-I_C relation for different I_b. Red trace is the optimum steady state for *Q* point.

An important issue in the circuit design is the matching impedance with respect to the electronic element and the transmission line in the PCB. Therefore, the characteristic impedance (Z_0) for the microstrip line can be calculated using some physical and electromagnetic parameters as Eq. (1) shows [13].

$$Z_0 = \frac{120\pi\sqrt{\varepsilon_{eff}}}{\frac{W}{H} + 1.393 + 0.667\ln\left(\frac{W}{H} + 1.444\right)} \tag{1}$$

where W is the width, H is the dielectric thickness and ε_{eff} is the effective dielectric constant. In particular, Eq. (1) is only suitable for microstrip satisfying the relation (W/H > 1). However, to optimize this matching, a transmission line calculator was used where the transmission line type, length and dielectric material characteristics were selected to produce a $Z_0 \approx 50\ \Omega$ and a minimum capacitance and inductance (see Fig. 5). Due to the high power demand of the circuit, a Trace Width analysis was performed in order to calculate the minimum trace width based on the Root Mean Square (RMS) electric current in each electrical path. Fig. 6 shows the Printed Circuit Board (PCB) layout based on the aforementioned parameters and Fig. 7 shows the three-dimensional view of the PCB. The *UltiBoard* software was used for the PCB designs.

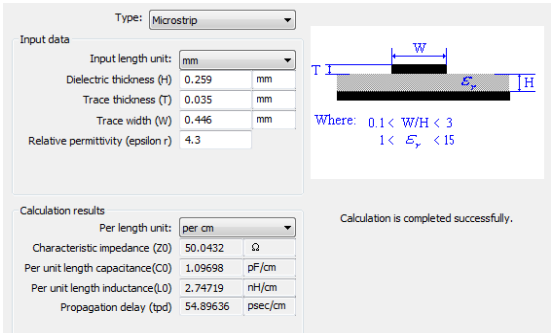

Fig. 5 Transmission line calculator in order to determine the characteristic impedance based on particular physical features of dielectric material and microstrip.

By using the matching circuits IMN and OMN shown in Fig. 2 and 3, the input and output impedances of the PA and LNA are obtained as follows: for PA, Z_{in} = 50.1 Ω and Z_{out} = 49.48 Ω, while for LNA circuit, Z_{in} = 49.3 Ω and Z_{out} = 45.05 Ω. The good impedance matching was performed using L-section networks (i.e. using an inductor and a capacitor), however, the bandwidth and gain are an important trade-off considered in the complete design.

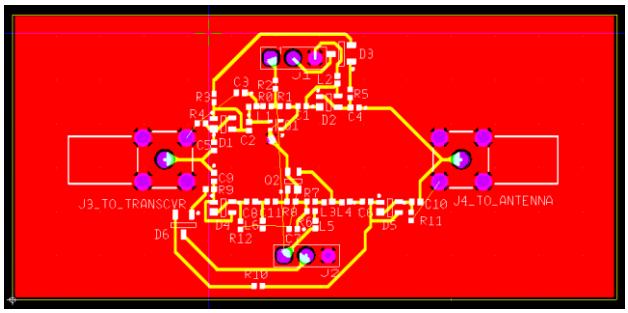

Fig. 6 PCB layout using C0402 packaging in each electronic element.

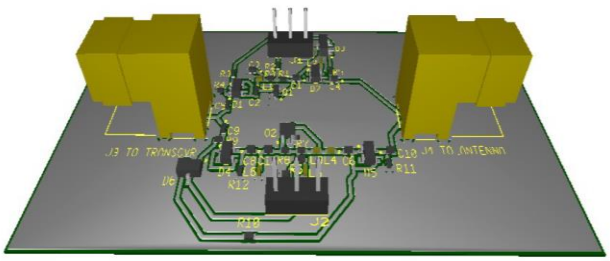

Fig. 7 3D view of Printed Circuit Board layout.

3. Simulation Results

Fig. 8 shows the simulation results of the *S*-parameters for the reception mode. The S_{12} value means that there is a high transmission power ratio (≈ 21 dB) of the complete circuit (LNA+PA+ High speed RF switch), while the S_{22} value (≈ -19 dB) and the S_{11} value (≈ -21 dB) means a good matching performances achieved in the input and output ports, respectively, in the reception operation mode. The S_{21} (≈ -27 dB) has an adequate electrical performance of isolation between input and output ports.

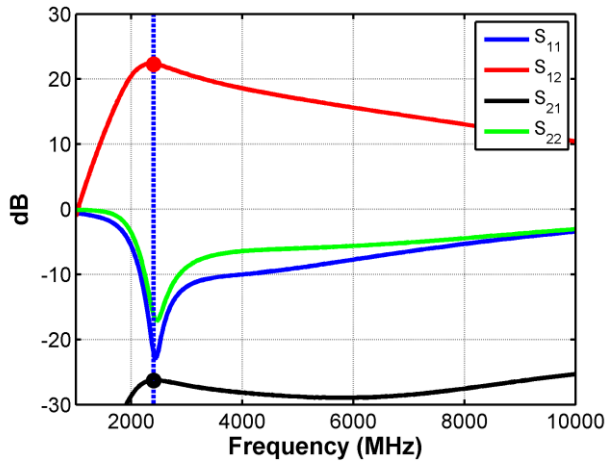

Fig. 8 Performance of the PA-LNA scheme in the reception mode (port #2 is the input and port #1 is the output).

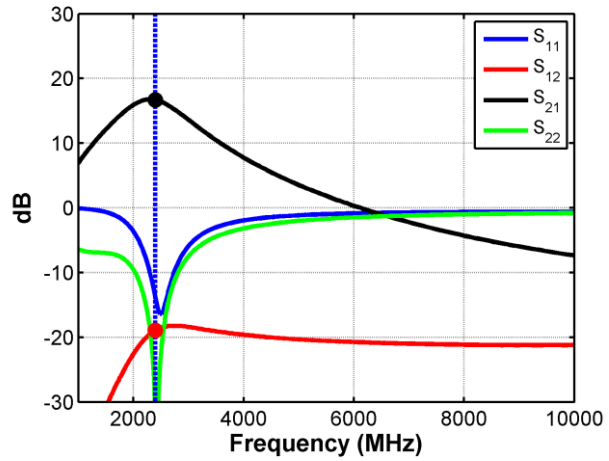

Fig. 9 Performance of the PA-LNA scheme in the transmission mode (port #1 is the input and port #2 is the output)

With respect to the measurements of the *S*-parameters in the transmission mode (see Fig. 9), S_{21} and S_{12} are the most important because they describe the transmitted and the reflected level signal (≈ 18 dB and ≈ -19 dB, respectively). In addition, Fig. 10 shows the performance of NF and gain (G) depending on the temperature variation at 2.4 GHz. The NF measurement is ≈ 0.6 dB and gain is ≈ 21 dB for 27 °C.

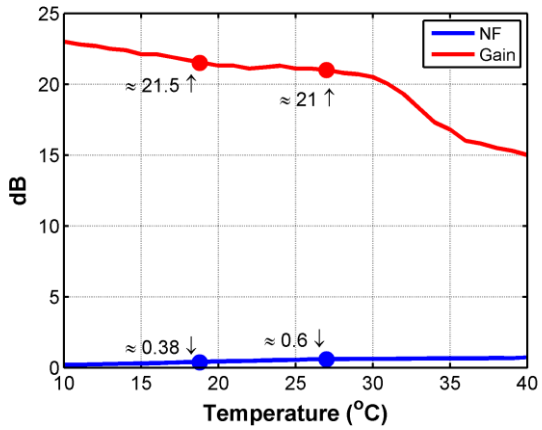

Fig. 10 NF and gain of the PA-LNA scheme in transmission mode (slot #1) at 2.4 GHz with temperature variations.

In addition, NF and G parameters were measured at 18.8 °C (i.e. 292 °K, temperature standard). In this case, NF is ≈ 0.38 dB and G is ≈ 21.5 dB.

4. Conclusion

This paper presented a transceiver circuit that has good performance parameters considering *S*-parameters, noise figure and gain based on the detailed design for IMN and OMN. The plug-and-play feature imposes an easy way to extend the coverage of different traditional wireless systems based on the IEEE 802.15.4 standard. It is important to clarify that the principal objective of the proposal is to increase the distance of the communication link of systems based on IEEE 802.15.4. Therefore, although conventional and commercial transceivers perform other processes (e.g. digital-to-analog converter, frequency synthesizer, among others), our proposal only focuses on improving the transmission and reception mode without considering modulation, synchronization, coding, encryption among others schemes. In particular, the analysis for the PCB design is based on microstrip transmission lines, although a ground layer is added in order to improve the performance. Due to the above, it is possible to confuse the transmission lines shown in Fig. 7 as a conventional coplanar waveguide (CPW). In fact, the impedance analysis is not performed considering a CPW. Currently, we have a first prototype that uses FR4 dielectric material in order to perform some Accelerated Life Testing (ALT) and Technical Operating Production (TOP). In addition, the transceiver circuit has been manufactured using a flexible dielectric material and other types of transmission lines in order to enhance the electronic performance.

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