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SINGLE EVENT TRANSIENTS MONITORING AND DIAGNOSTIC IN FPGA

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Abstract. *Analysis of single event transients (SETs) generated in field programmable gate arrays (FPGA) under heavy charged particles (HCP) irradiation and SET suppression methods is performed. The circuit for FPGA SET detection is designed for transients generated both inside FPGA and outside at package pin level. SET registration inside FPGA is carried out as an event when logical cell is switched. The SET control schematic circuit efficiency has been comparatively verified using heavy ion accelerator and picosecond focused laser source. SET in FPGA experimental results are presented and discussed.*

Key words: *high-performance systems, space radiation, single event transients, digital integrated circuits, FPGA, failures, HCP, VLSI, TMR*

1. INTRODUCTION

Development of high-performance systems, such as telecommunication technologies, orbit the group of Earth remote sensing, navigation and global positioning systems (Glonas, GPS, Galileo, Beidou) and require the usage of high-performance microelectronics devices. The main trend of high-performance systems design is data processing speed of the information flow increase. Data processing speed rise is obtained both by memory cluster growth and the range of integrated circuits (ICs) operating frequencies increase. This trend in the development of high-performance systems require the usage of microchips with fewer than 250 nm design rules that leads to smaller supply voltage and growth of elements density on a chip.

One of the main components used to create high-performance systems are programmable logic gate arrays (FPGA). A distinctive feature of FPGAs is the possibility of easy reconfiguration of the logical structure within the framework of the logical elements basis implemented in FPGAs. Modern FPGAs are available as elementary logical structures implemented in the basis of look up tables (LUT) cells constituting FPGAs and complete

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built-in IP units, such as memory, phase locked blocks (PLL), codecs and decoders for various purposes, microcontroller and microprocessor cores, etc. Due to these unique characteristics, FPGAs are used to implement autonomous high-performance systems in on-board space equipment. However, in real operating conditions ionizing radiation from space environment impacts all electronic devices and it may lead to IC upsets, failures and damages.

Space environment induces two main ionizing radiation effects in microelectronic devices: total ionizing dose (TID) [1] – [5] and single event effects (SEE) [30] – [32]. TID effects cause the degradation of IC element parameters associated with the accumulation of radiation-induced charge in silicon dioxide insulator that leads to MOS transistors threshold voltage shift and the corresponding leakage current increase at the edge of NMOS transistors. The design rules decrease causing the corresponding gate silicon dioxide thickness to decrease and therefore TID effects in MOS transistors are not of great importance for modern sub-micron devices.

SEE due to HCP are crucial to ICs. Such SEE as single event upsets (SEU) and single event transients (SET), are associated with digital elements logic state inversion possibility. Modern design rules make it possible to increase operation frequency and to reduce IC element input capacitance. Higher operation frequency rise up the probability of SET on data lines that cause a real data corruption. Small input capacitance of IC element leads to less linear energy transfer (LET) threshold that can change logic state of digital element. If we assume a typical submicron process capacitance of 0.1- 0.4 pF then the induced charge can form a voltage pulse up to volts (for a typical 1.2 V power supply voltage), which can lead to a change in the logic state of a digital circuit element. In connection with this reasons the dominating of SET over SEU in modern circuits is the most significant effect for high reliability system design for space applications.

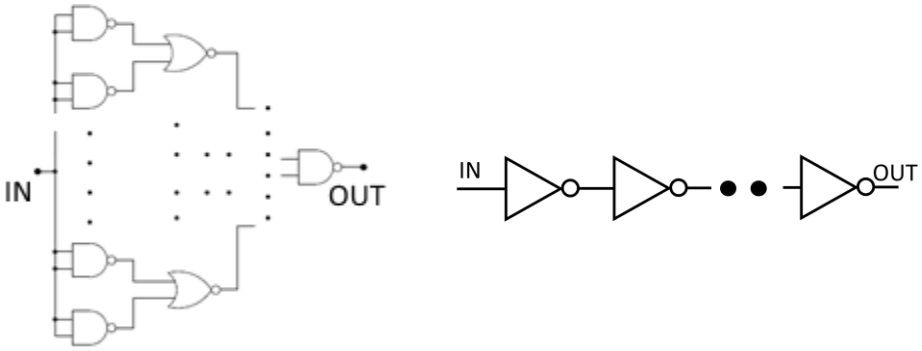
The main goal of this work is to demonstrate how SETs in FPGA are able to be registered and the possible consequences of SET. The paper analyses SET research method and appropriate ground facilities. The obtained original experimental results of SETs in FPGA are described.

2. TYPICAL SCHEMES OF SETS EFFECTS RESEARCH IN DIGITAL ICS

SET effects modeling in different types of asynchronous logic elements combinations are presented in [6] – [9]. The presented data analysis makes it possible to conclude that authors use two basic combinations – parallel (Fig. 1.a) and consistent (Fig. 1.b) chain of logic circuit elements.

For analog ICs SETs authors of [10], [11] adduce amplitude and time duration as significant characteristics. For digital SETs that kind of characteristic is redundant. The most important question for real system is how SETs propagate through internal IC elements to external IC package pins and how those SETs are latched by IC trigger structures. Taking that into account, logic chain variants presented in Fig. 1 are not sufficient for SET research in digital ICs. Presented logic chains give us information about SET propagation to an external pin, as well as about SET time duration and amplitude, but no information about latching SET by internal trigger structures.

SETs simulation for sub-micron process is presented in [12]. TCAD results show that SET duration must be from tens to hundreds of ps for submicron process (see Fig. 2), that is in good agreement with experimental results.



a. parallel chain b. consistent chain

Fig. 1 Examples of asynchronous logic elements chains used for SETs investigation

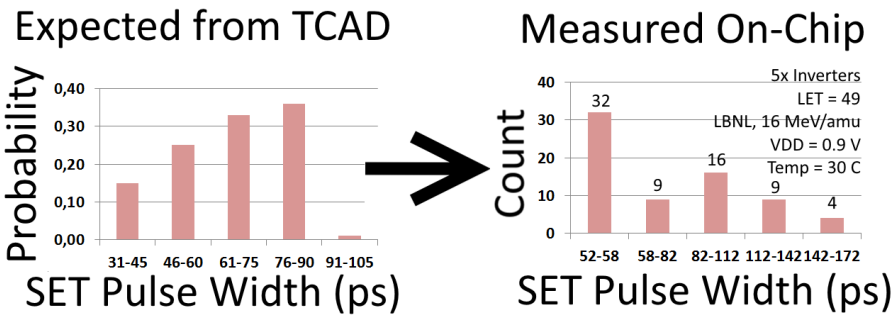


Fig. 2 TCAD and on-chip measured time duration of SETs in sub-micron process [12]

3. FPGA CONFIGURATION FOR SETS MONITORING AND DIAGNOSTICS IN GROUND EXPERIMENTS

Fig. 3 presents the proposed schematic diagram for monitoring and diagnostics of SET in FPGA. The investigated SET generation occurs in the chain of asynchronous logic (in the example it was considered that the chain consists of 195 inverters connected in a series). The choice of the number of inverters in the chain is a compromise solution. On the one hand, a large number of inverters increase the probability of the SET. On the other hand, it is necessary to take into account the logical capacity of the IC. Thus, the number of inverters in the chain must be as high as possible. The external signal 'inv_in' specifies the inverters chain output signal logical state. The chain output is connected directly to an external package pin of the IC under test (signal 'inv_out') and also connected to clock inputs of three D-flip-flops. Connecting the output of the inverters

chain to three D-flip-flops allows us to monitor the fact of the SET origin that can switch the logical state of the IC digital elements. The SET formation fact is monitored by analyzing the triple measure redundancy (TMR) element output state which is connected to the outputs of D-flip-flops, as well as by the state of 'the tmr_out [2..0]' signals, which are the outputs of D flip-flops connected to the external package pins of the IC. Ion accelerator experiments suggest that all ICs elements are under irradiation unlike on the focused laser source when irradiation influenced to the limited area of the chip. In the experiments on focused laser source the limited area does not include the TMR element. The used TMR element in that scheme makes possible to separate SET in the inverters chain and SEU in D flip-flop. The output 'inv_out' is used to control the form of the transient process that has propagated to the external pin of the investigated IC. The observation of a SET form is performed using an oscilloscope that records signals at the ICs' package pin point where the signal line 'inv_out' is connected.

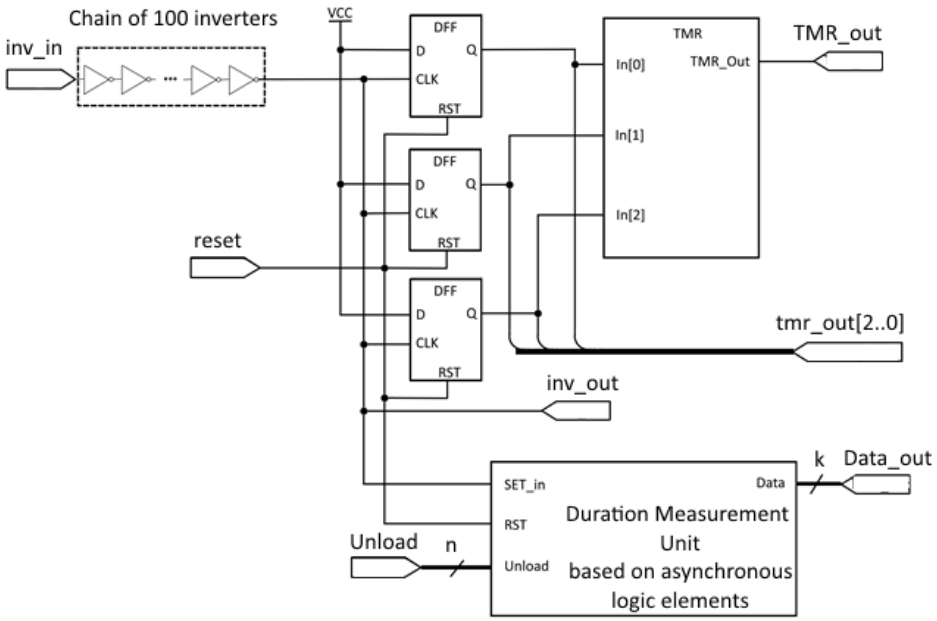


Fig. 3 The schematic diagram for SETs in FPGA monitoring and diagnostics

Transient registration is based on the following algorithm: HCP ionize the part of IC semiconductor, the induced charge is collected by active element region in the inverters chain, and collected charge switches the logic state of inverter and generates voltage pulse at the inverters chain output. The generated short-time transient process is detected by the clock inputs of D flip-flops as the synchronization signal; after that the input data (logical '1') of D flip-flops is latched. After the SET occasion an external reset (the signal 'reset') is sent and the outputs of the D flip-flops take the state '0' as a result.

SET registration diagram (see Fig. 3) assumes the presence of the block (Duration Measurement Unit - DMU) responsible for analyzing the duration of SET (see Fig. 4). DMU is formed by the composition of logical elements available in IC under test. DMU

allows to measure the SET duration which is based on the logical element switching time within the IC composition. As it is shown in Fig. 4 the DMU consists of two parts. The first DMU part is responsible for SET duration which is measured in quantity of the switched logic elements. The second DMU part is a functional block which downloads data about the switched logic elements.

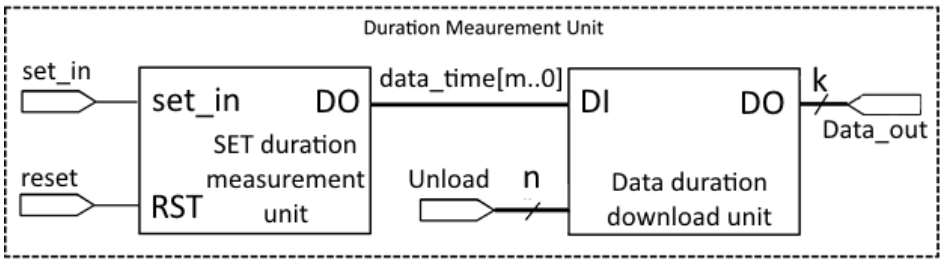


Fig. 4 SET duration measuring diagram based on logic elements.

DMU schematic diagram is presented in Fig. 5. One can see the SET duration measured by the number of switched inverters during the time of the transient process in the logical ‘1’ state. The feedback made on the signal ‘SET_in’ on the ‘AND’ element allows to exclude the accidental latching of the state '1' by the D flip-flop in case of the SET occurrence in the duration measurement circuit.

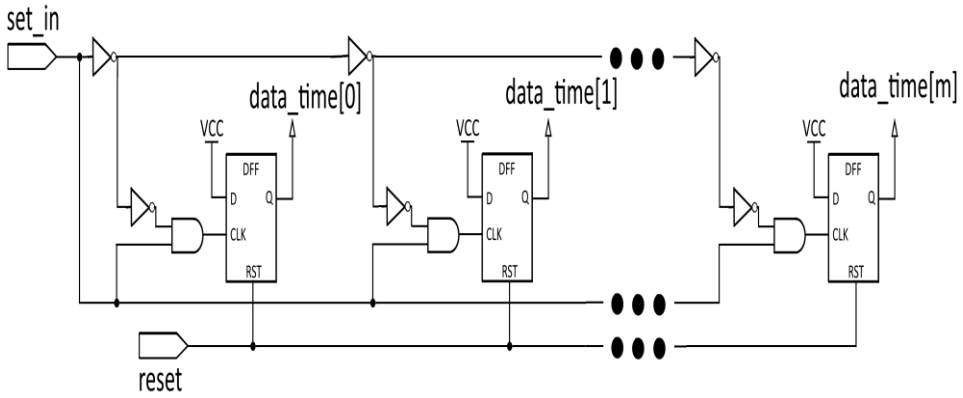


Fig. 5 DMU schematic diagram.

The scheme for SET duration data downloading can be realized in various ways. If the unit is implemented as FIFO with parallel loading, the signal community ‘UnLoad’ will represent the following form: the parallel loading signal - ‘Load", the signal of the data load permission is ‘CE’, the clock signal is ‘CLK’. For example, it is also possible to implement in the form of a multiplexer. In this case signal ‘UnLoad’ is group of signals for addressing inputs of the multiplexer (see Fig. 6). Other variants of implementation are also possible.

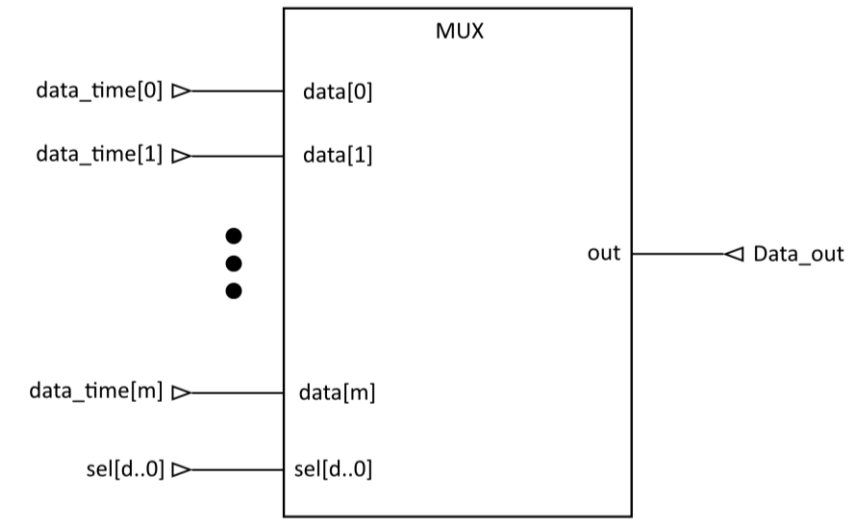


Fig. 6 SET duration data downloading unit in MUX realization.

4. Experimental VERIFICATION OF SET'S IN FPGA Monitoring Setup

Verification of the proposed scheme for SET monitoring was carried out at: the cyclotron of heavy short-range ions U-400M (JINR, Dubna, Russia) [13] and the source of focused laser radiation PIKO-3 (SPELS, Moscow, Russia) [14], [15]. The research was carried out for three types of FPGAs built in Antifuse process and one CMOS ASIC in 180 nm design rules. In future we are going to investigate SETs in a test chip in 90 nm design rules. SETs were detected in all devices under test (DUT) and in all experiments. The most interesting results have been found in the first type of irradiated FPGA, in other DUTs regular forms of SETs (traditional bell-shaped form) were registered. SETs with durations from hundreds ns to several microseconds and essential amplitude fluctuations were detected with U-400M ion accelerator. The registered SETs amplitude was found to be from hundreds of mV to the supply voltage limit. SETs were registered under ions with LET from 7 MeV • cm^2 / mg (Si) to 69 MeV • cm^2 / mg (Si) (all available ion LETs at the facility).

At the second research stage the proposed Antifuse FPGA SETs investigation method was verified using the picosecond laser source PIKO-3. The irradiation was carried out from top side of IC chip by laser radiation with 1.064 μm wavelength. At the initial stage of the experiment, the chip was scanned with the step of 50 μm and energy of 300 nJ. In the process of scanning the chip's surface SETs were monitored at the DUT external pin (line 'inv_out'), at the output line from TMR (line 'TMR_out') and at D flip-flops three output signals (tmr_out[2..0]). After chip surface scanning the particular places on chip layout which was dedicated to SET origin was localized and the stability of the registered SETs generation was confirmed.

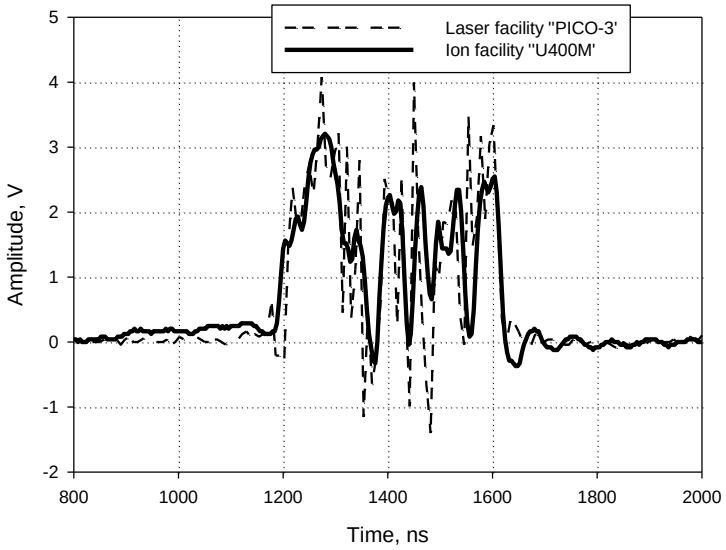


Fig. 7 Laser and ion facilities SETs comparison

The performed laser experiments gained the following results:

- Places in FPGA layout were found where transients are generated;
- It was established that all the formed SETs lead to the triggering of TMR;
- The SET origin energy threshold in picosecond focused laser test was determined as 200 nJ.

The comparison of the registered transients forms and durations obtained within the ion accelerator and focused laser tests (see Fig. 7) demonstrates that laser methods are applicable for investigating single events in digital VLSI [16] – [18] and their results are in a good agreement with heavy ion accelerator results.

Some abnormal durations and forms of SETs observed were found to be associated with the discharging of HCP's induced charge through large resistance in the disabled RAMs' cells in antifuse mode. In the next FPGA chip versions this design mistakes was corrected and abnormal SETs disappeared.

Also in accelerator experiments SEU in RAM and SET effects in one type of FPGA were investigated. Table 1 presents the summary information of SET and SEU control. Fig. 8 demonstrates experimental SET and SEU cross-section.

The following conventions are used in Table 1:

- LET [MeV×cm^2/mg]– Linear Energy Transfer.
- F [1/cm^2] – Fluence ion irradiation accumulated during the session
- σ_{SET} / σ_{SEU}[cm^2/gate / cm^2/bit] – Cross section SET/SEU measured for one inverter/bit.
- DUT – Device Under Test
- N_{SET} / N_{SEU} – Number of SET/SEU registered during the ion irradiation session

Table 1 Experimental results of SEU and SET control in FPGA

ION	LTE, MeV×cm²/mg	DUT	F, 1/cm²	N_{SET}	σ_{SET}, cm²/gate	F, 1/cm²	N_{SEU}	σ_{SEU}, cm²/bit
Xe	≈ 65	1	7,2E+06	101	7,1E-08	6,3E+06	72	4,5E-08
		2	7,0E+06	120	8,6E-08	6,1E+06	55	3,6E-08
Kr	≈ 40	1	1,2E+07	103	4,3E-08	4,2E+06	25	2,4E-08
		2	1,2E+07	105	4,4E-08	4,2E+06	30	2,9E-08
Ar	≈ 17	1	2,7E+06	3	6,8E-09	2,7E+07	49	7,2E-09
		2	2,5E+07	21	4,3E-09	2,5E+07	55	8,7E-09
		3	2,3E+07	11	2,5E-09	-	-	-
Ne	≈ 7	1	1,6E+07	0	3,7E-10	-	-	-
		2	1,6E+07	0	3,7E-10	-	-	-
		3	1,7E+07	0	3,7E-10	-	-	-

As can be seen from Fig. 8 even in asynchronous combination logic in static mode SET can occur with frequency near the SEU frequency. This means that it is important to control not only SEU but also SET. Under adverse design of synchronization lines in FPGA (for example) it is possible that SET has a significant influence on the functioning of the device as a whole.

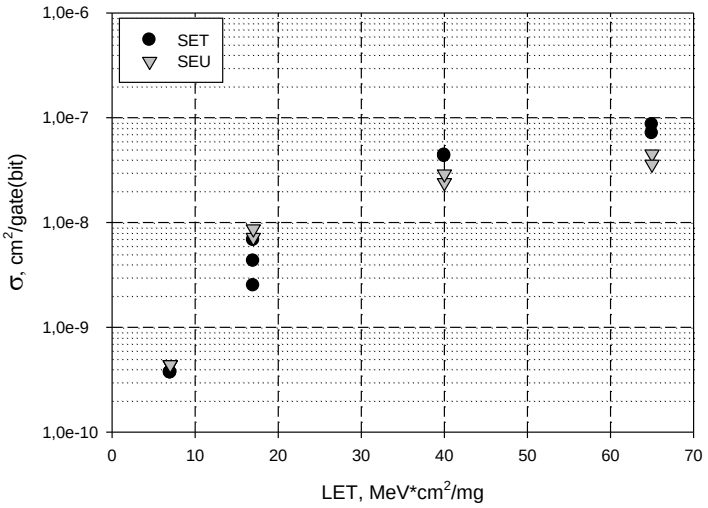


Fig. 8 SET (σ_{SET}) and SEU (σ_{SEU}) cross section vs heavy ions LET

5. CONCLUSIONS

SETs research in digital ICs is an important aspect for fault-tolerant system design for space application. The presented experimental results demonstrate that SETs are generated under the influence of HCP in modern VLSI, which are capable to induce false triggering of combinational circuits that cause change to the stored information in the trigger structures, i.e. SET turns into SEU. The amplitude and time characteristics prediction of generated SETs is necessary to work out SET filtering and correction circuits for space application.

The experimental comparative results obtained at the heavy ion accelerator U-400M and the focused picosecond laser radiation source PIKO-3 are in good agreement. The use of laser source for SET research allows to localize semiconductor structures responsible for the SETs generation and their conversion to SEU. The focused picosecond laser sources, especially in combination with heavy ion accelerator is a very informative and efficient facility of SET experimental research and prediction.

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