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A NOVEL SUPPLY VOLTAGE COMPENSATION CIRCUIT FOR THE INVERTER SWITCHING POINT

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Abstract. *The present work proposes an innovative circuit that is able to compensate the inverter switching point voltage variation due to supply voltage change. The circuit is designed to work for a 1.6V to 2V supply voltage range. The operation principle includes the back gate effect and an original transistor switching.*

Key words: *adaptive threshold, inverter, back gate effect*

1. INTRODUCTION

Increasing modern circuits working frequency precision and low current consumption are important prerequisites for a modern design. The logic gate delays are used for periodical signal generation and time synchronizing. At high speed, the gate delay approach is to be considered, due to its low power consumption, reduced area, simplicity in design and large integration.

When using logic gates as delays, the gate delay is proportional with the supply voltage variation.

For a ring oscillator case, the frequency lowers as the supply voltage rises due to the fact that the stage capacitors are charging to higher voltage.

The inverter schematic is exposed in Figure 1.

The usual approach is to design the inverter switching point to be half of the supply voltage. The switching point of the inverter is denoted with V_{SP}.

The transfer characteristic for the former stated case is shown in Figure 2.

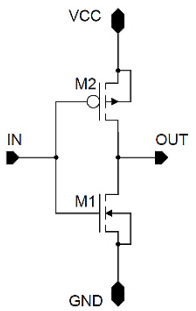

Fig. 1 CMOS inverter schematic

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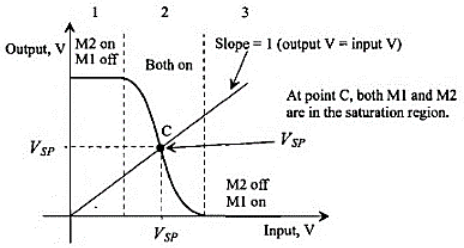

Fig. 2 CMOS inverter transfer characteristic [1]

In region 1 of the transfer characteristic of the inverter M2 is in on state and M1 in off state. As the input voltage rises over the M1 threshold voltage, the transistor enters conduction state and M2 remains in on state. This is represented as the entering point in region 2. As the input voltage further increases, M1 turns on completely. At half of the second region represented with C is the switching point. In the second region, both transistors are in saturation state.

As the circuit is leaving the second region, M2 transistor starts to turn off and, eventually, it reaches the full off state as it enters the third region.

For the design of half the supply voltage switching point, both devices have the same drain current. Under this assumption, the next equation can be written 1 [1]:

$$\frac{\beta_n}{2}(V_{SP}-V_{THN})^2=\frac{\beta_p}{2}(V_{DD}-V_{SP}-V_{THP})^2 \tag{1}$$

After some equation processing, one can find equation 2 [1] which calculate the switching point voltage of the inverter; β_n and β_p are the NMOS and PMOS transistor transconductances, V_{THP} and V_{THP} are the PMOS and NMOS device thresholds:

$$V_{SP}=\frac{\sqrt{\frac{\beta_n}{\beta_p}}\cdot V_{THN}+(V_{DD}-V_{THP})}{1+\sqrt{\frac{\beta_n}{\beta_p}}} \tag{2}$$

The ratio between the PMOS and NMOS devices geometry can be estimated using equation 3, where X is a factor between 2 and 4, depending on the technology used:

$$(W/L)_N=X\cdot(W/L)_P \tag{3}$$

2. CONTROLLING THE INVERTER SWITCHING POINT

If the inverter is at the switching point, Rp1 and Rp2 form a resistor divider. The output resistance of the NMOS and PMOS devices are given by equations 4 and 5, λ is the body effect parameter:

$$R_{ON} = \frac{1}{\lambda \cdot \frac{\beta_n}{2} \cdot (V_{GS} - V_{THN})^2} \tag{4}$$

$$R_{OP} = \frac{1}{\lambda \cdot \frac{\beta_p}{2} \cdot (V_{SG} - V_{THP})^2} \tag{5}$$

Continuing with the resistor divider analogy, the inverter switching point is given by the following equation:

$$V_{SP} = \frac{R_{ON}}{R_{tot}} \cdot V_{DD}, R_{tot} = R_{ON} + R_{OP} \tag{6}$$

An increase of the threshold of the NMOS device will result in a decrease of the drain current and an increase of the device resistance. On the other hand, an increase of the absolute value of the PMOS threshold will result in an increase of the device current and a decrease of the device resistance.

The decrease of the PMOS resistance will lead to the lowering of R_{tot}; the value of V_{SP} will rise. On the NMOS side, increasing the device resistance will lead to the increase of R_{tot}; V_{SP} will go down. These statements are expressed in a simplified manner in equation 7 and 8:

$$V_{THN} \uparrow \Rightarrow I_{DN} \downarrow R_{DSN} \uparrow \Rightarrow V_{SP} \downarrow \tag{7}$$

$$|V_{THP}| \downarrow \Rightarrow I_{DP} \uparrow R_{DSP} \downarrow \Rightarrow V_{SP} \uparrow \tag{8}$$

The transistor threshold can be modified using the back gate effect, by regulating the bulk voltage accordingly, and sensing the threshold on an inverter with the output tied to the input. As stated in [2], the transistor threshold is influenced by the bulk voltage according to equation 9:

$$V_{TH} = V_{TH0} + \gamma \cdot (\sqrt{|2\Phi_f - V_{SB}|} - \sqrt{|2\Phi_f|}) \tag{9}$$

In Figure 3, the inverter schematic with bulk control voltages and the intrinsic device diodes are shown.

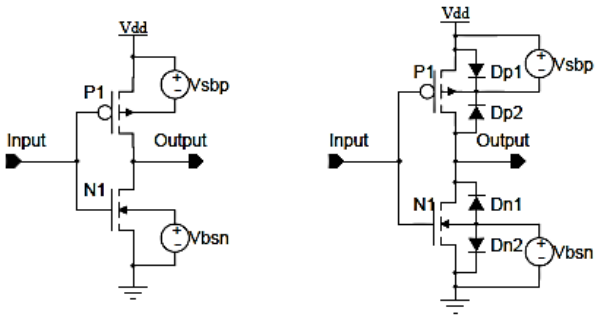

Fig. 3 Back gate controlled CMOS inverter

In normal operation, the bulk is tied to the source and diodes Dp1 and Dn2 are shorted out. The other two diodes, Dp2 and Dn1 are reversed biased [5] and only a small current crosses them. When the source bulk voltage is applied, diodes Dp1 and Dn2 become forward biased and, if the correct amount of voltage is applied on the bulk of the transistor, the diodes can enter conduction. This situation is illustrated in Figure 4.

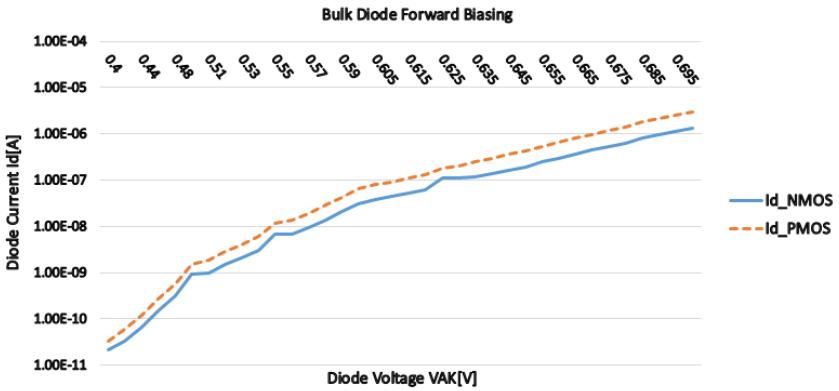

Fig. 4 Bulk diode forward biasing

As resulting from Figure 4, the maximum back bias voltage should not exceed 600mV. For the sake of safe design, the back bias voltage will be designed not to exceed 550mV.

The downside of bulk biasing is that across the forward biased bulk diode there will flow a small amount of current no matter how small the bulk voltage will be. Also, the NMOS device has to be isolated in a separate well. Regarding the PMOS transistor, this device is already isolated due to the NWELL in which it is constructed.

The good part is that the diodes will start to conduct when having a drop of at least 0.6V. Also, from the stand point of view of area, all the NMOS isolated devices can share the same well [5].

3. Adaptive Threshold Circuit

3.1. Modified inverter schematic

First the inverter supply voltage switching point variation must be evaluated. Then, the supply voltage range will be split into two domains, symmetrical around the centre value. For this particular case, the centre value for the supply voltage is 1.8V, the minimum and maximum being 1,6V and, respectively, 2V.

The switching point voltage will be increased for the low range of the supply and decreased for the high range. By referring to the original inverter schematic, at half the supply range the original switching point characteristic and the adjusted one will cross.

Simulations lead to the conclusion that the supply range is too large to be adjusted only by bulk regulation. Therefore, the approach of switching a part of the original transistors for each range has been taken into consideration.

The new inverter schematic is shown in Figure 5.

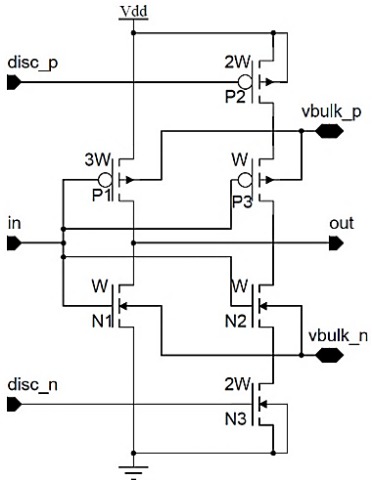

Fig. 5 Modified inverter schematic

A similar principle is proposed in [3]. This is done by using multiple fingers for the NMOS transistor. These transistors, are floating gate type, and need to have their threshold programmed. By programming or erasing, there is added or subtracted one or several NMOS devices. This method, although very effective, cannot be used to adjust continuously the inverter switching point.

The inverter is made out of transistors P1, P3, N1, and N2; without switching (P2 and N3 are conducting), P1 and P3 are acting as an equivalent PMOS transistor of 4W channel width, and N1, N2 as a NMOS transistor of 2W channel width. P2 and N3 transistors are in charge of disconnecting transistors P3, respectively, N2, in the regions where the inverter threshold cannot be adjusted only by bulk regulation. The two transistor used as switches, are controlled by signals disc_p and disc_n. P3 represents ¼ of the total PMOS width and N2 ½ of the NMOS width. The bulks are common and yet to be externally controlled for P1 and P3 pair, and N1, N2 pair.

By disconnecting P3 PMOS transistors (P2 is OFF), the inverter threshold will be lowered.

In the same manner, by disconnecting N2 NMOS transistors (N3 is OFF), the inverter threshold will rise.

The centre of the supply span is taken as reference. This is the reason that the 1.8 volt supply is the point where the circuit will switch from increasing the switching point voltage to decreasing it. That means that the circuit will switch from regulating the PMOS bulk voltage to regulating the NMOS bulk voltage. The regulation of both transistors bulks will not bring any functional improvement, because the effects are in opposite directions.

Switching P3 off (which has ¼ of the total PMOS width) will decrease the switching point voltage. On the other hand, switching N2 off (which has ½ of the total NMOS width) will increase the switching point voltage. This is the reason for the extra two sub domains that control the switching of P3 and N2; this brings a rough adjustment where

the body effect can no longer tune the V_{SP} variation. To describe better the functionality of the circuit, the voltage domains are exposed in Figure 6.

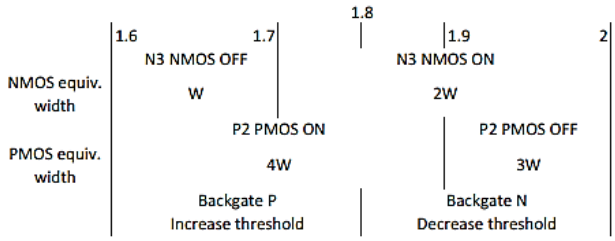

Fig. 6 Threshold adjustment principle

Perfect symmetry of the domains is desired but it would be very hard to obtain. The goal is to layout the complementary PMOS and NMOS transistors as a number of identical fingers having the same dimensions. Also, the width of the composing finger should be a fractional number but containing only the first digit after the point. There is no use to try to obtain high precision when switching the extra transistors, because their effective length and width will change due to process variation. In the end, the maximum bulk voltage will be different between the PMOS and NMOS devices. This is also due to different mobility and geometry of the complementary devices. In the end, the importance of this circuit is to obtain a threshold with a low variation and to keep the bulk voltages under the maximum limits.

The circuit needs two regulation loops, one for the PMOS bulk and one for the NMOS bulk and a supply voltage monitoring block. The supply monitor will be composed out of 3 independent circuits, each signalling one of the voltage intervals shown in Figure 6.

3.2. Adaptive threshold circuit

The proposed adaptive threshold circuit is exposed in Figure 7.

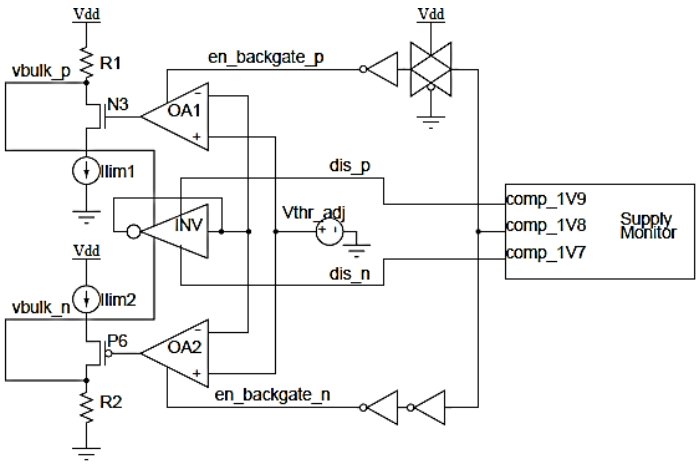

Fig. 7 Adaptive threshold circuit

The bulk voltages are generated using regulated current to voltage converters [6]. The centre inverter, enclosing the schematic exposed in Figure 5, is used as switching point reference. For regulating the PMOS bulk voltage is used the operational amplifier OA1, NMOS transistor N3, resistor R1 and Ilim1 current source (this one being a client form the general biasing mirror). OA1 compares the switching point voltage of inverter INV with the Vthr_adj voltage. If V_{SP} is lower, the vbulk_p voltage will be increase and the threshold will go up.

On the other hand, the NMOS bulk voltage is regulated by OA2, PMOS transistor P6 and current source Ilim2. OA2 compares the V_{SP} value with Vthr_adj voltage and regulates the vbulk_n node voltage in order to decrease the threshold.

Both Ilim values are set to 5uA so that the voltage drop across R1 and R2 would be limited to about 500mV. With a 10% variation of the bias current, the maximum bulk voltage will not exceed the safe operation area, depicted in Figure 4.

The value for the Vthr_adj voltage is the inverter switching point at half the supply domain; in this case for a supply of 1.8V it will be 0.75V. Setting this parameter is critical, in order to obtain the lowest variation.

The supply monitor block has three outputs, comp_1V7, comp_1V8 and comp_1V9. The comp_1V7 controls the dis_n signal of the inverter, disconnecting the extra NMOS transistor for a supply voltage under 1.7V and connecting it when the supply exceeds this limit. Comp_1V9 signal controls the dis_p signal, keeping the extra PMOS connected for supply voltages under 1.9V and disconnecting it when the voltage limit is exceeded.

Comp_1V8 controls which of the PMOS or NMOS bulks are regulated. For supply voltages under 1.8V, the PMOS bulk is regulated, and over 1.8V, the NMOS bulk is regulated. The operational amplifiers have basically the same schematic, the only difference is that OA1 pulls down the output when disabled and OA2 pulls is up. This is done in order to disconnect N3 and P6 when the OPAMPS are off. In this manner, the PMOS bulk will be pulled up, and NMOS bulk pulled down, by R1 and R2 resistors.

The supply monitor schematic is exposed in Figure 8.

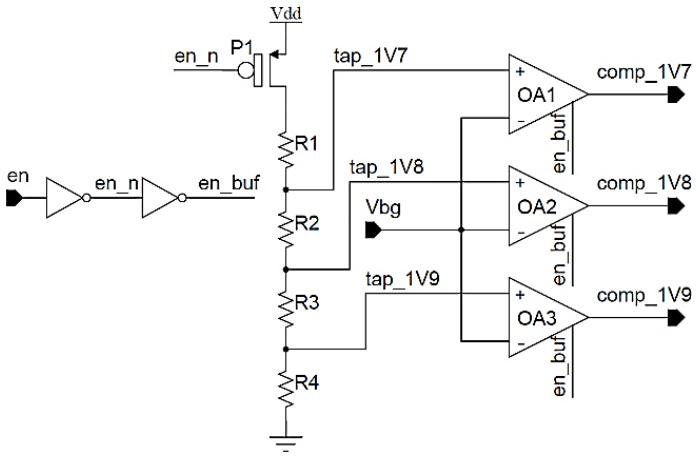

Fig. 8 Supply monitoring circuit

The resistor divider has been drawn as four independent resistors (normally it contains several resistor fingers, each finger hasthe same number of squares and resistance value); the bias for the operational amplifiers is omitted in the picture. Each of the amplifiers is using an external 1uA bias current.

The resistor divider composed out of R1, R2, R3, R4 and the disabling P1 transistor, reduces each supply voltage threshold to the value of the system voltage reference V_{bg}=1.2V. The three OPAMPS, OA1, OA2 and OA3 compare the two values (the certain tap of the resistor divider and the bandgap voltage reference) and switch the output to logic 1 when the resistor tap voltage exceed the bandgap voltage value. P1 transistor has the role of switching off the resistor divider, in order to reduce current consumption when the circuit is disabled. In simulation, the reference voltage is provided by an ideal voltage source.

The schematic of comparator is depicted in Figure 9.

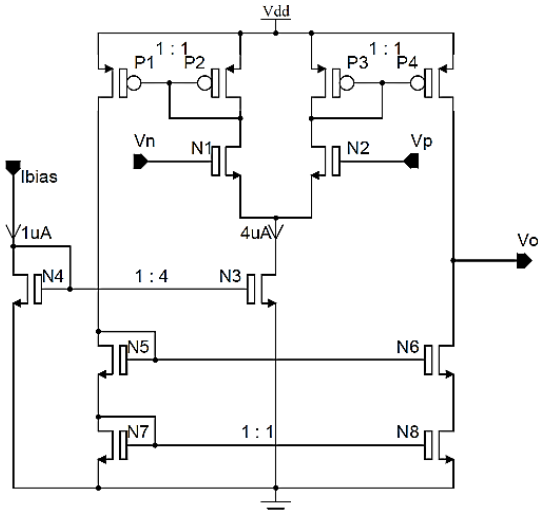

Fig. 9 Comparator schematic

The comparator uses a trans-admittance amplifier. The topology was chosen due to the capacitive load driving capability. P2 and P3 PMOS transistors act as active loads for the differential input stage. The input offset is optimised by providing high matching between the differential pair bias currents.

This is done by using a topology that offers high precision biasing for the differential input stage of the comparator. To enhance even more the schematic, the NMOS current mirror (N7-N8) which regulates the current between the active load current mirrors (P1-P2 and P3-P4) is cascaded with transistors N5 and N6. The cascode topology also enhances the output resistance of the block.

3. Simulation, Results and Discussion

Figure 10 exposes the circuit operation.

The source-bulk and bulk-source voltages define the two operation modes.

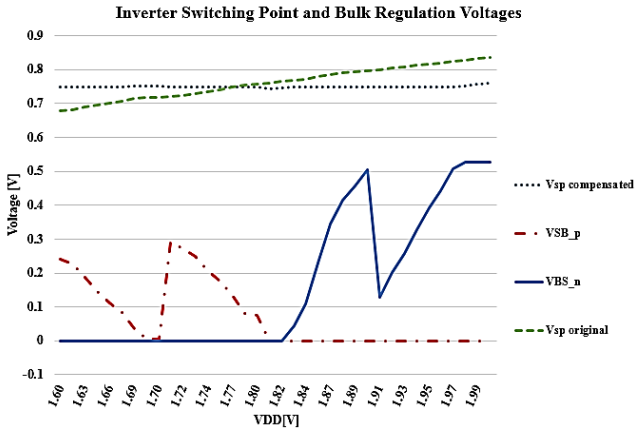

Fig. 10 Inverter switching point and bulk voltages simulation

The regions where the back bias increases (PMOS) and decreases (NMOS) rapidly represent the switching points for the extra transistors. From simulation, the inverter switching point can be tuned by body effect only between 1.7V and 1.9V supply voltage. For the NMOS bulk regulation, the bulk voltage almost reaches the maximum safe operation voltage.

The simulation was done for a 1.6-2V supply voltage sweep, using Cadence spectre. The temperature set is 27ºC, and it used the typical corner for simulation. Finer adjustments can be made. For example, the extra NMOS that is disconnected can have the width a bit lower. Although this adjustment is possible, it would require to work with transistor fingers of 0.5W or smaller, reaching the minimum technological size. Comparing the original threshold with the adjusted one, there is to conclude that the circuit is doing its job properly.

Figure 11 presents the difference between the original inverter, with all transistors working and no bulk regulation, and the same inverter that has both bulk regulation and transistor switching.

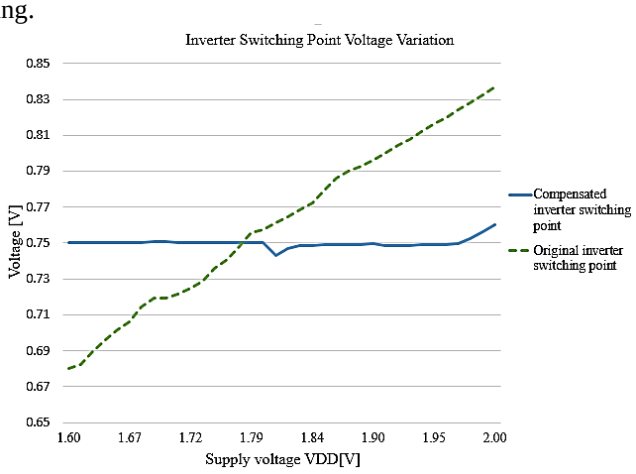

Fig. 11 Comparison between the original and improved inverter switching point

The two characteristics are close to meet on the 1.8V supply voltage value. There is a little offset due to the fact that the original inverter had the switching point a bit higher than 0.75V at VDD=1.8V and the regulated value was chosen to be 0.75V. Also, when reaching the upper part of the supply range, the NMOS bulk regulation cannot cope with the variation anymore. Same thing happens around half the designed supply voltage but the threshold decreases.

The maximum values for some important signals, in the case of the, nominal, 25ºC simulation, are underlined in Table 1:

Table 1 Circuit relevant signals absolute values for the nominal corner

	Vsp_adj	Vsp_orig	VSB_p	VBS_n
nom(VDD=1.8V)	0.7504	0.7572	0.0743	0
min	0.7433	0.6801	0	0
max	0.7601	0.8368	0.2902	0.5282
delta	0.0168	0.1567		
delta[%]	2.24	20.7		

The switching point value in the table, represent the total variation reported to the central 1.8V supply voltage value (0.75V). The adjusted switching point variation is almost ten times lower than the original one. The overall technological corner variation is depicted in Table 2.

Table 2 Inverter switching point - Overall corner variation

	Max. Vsp variation [%]			
	Corner	fast	slow	typical
Temp[°C]	-40	3.59	4.08	3.67
	25	3.25	3.61	3.36
	85	3.44	3.71	3.51

Detailed corner simulation results are underlined in Table 3 and Figure 12.

Table 3 Inverter switching point - Technological corners simulation results

Temp. [°C]	-40					25					85				
Corner	fast	fast_hh	fast_hl	fast_lh	fast_ll	fast	fast_hh	fast_hl	fast_lh	fast_ll	fast	fast_hh	fast_hl	fast_lh	fast_ll
min. [V]	0.7409	0.7326	0.7326	0.7484	0.7484	0.7389	0.7389	0.7389	0.7478	0.7478	0.7474	0.7375	0.7375	0.7481	0.7481
max. [V]	0.7667	0.7595	0.7595	0.7736	0.7736	0.7633	0.7545	0.7545	0.7717	0.7717	0.7636	0.7531	0.7531	0.7739	0.7739
delta [V]	0.0258	0.0269	0.0269	0.0252	0.0252	0.0244	0.0156	0.0156	0.0239	0.0239	0.0162	0.0156	0.0156	0.0258	0.0258
delta[%]	3.44	3.59	3.59	3.36	3.36	3.25	2.08	2.08	3.19	3.19	2.16	2.08	2.08	3.44	3.44
Corner	slow	slow_hh	slow_hl	slow_lh	slow_ll	slow	slow_hh	slow_hl	slow_lh	slow_ll	slow	slow_hh	slow_hl	slow_lh	slow_ll
min. [V]	0.7472	0.7391	0.7391	0.7491	0.7491	0.7487	0.7434	0.7434	0.749	0.749	0.7483	0.7401	0.7401	0.7487	0.7487
max. [V]	0.773	0.7658	0.7658	0.7797	0.7797	0.7679	0.7593	0.7593	0.7761	0.7761	0.7665	0.7563	0.7563	0.7765	0.7765
delta [V]	0.0258	0.0267	0.0267	0.0306	0.0306	0.0192	0.0159	0.0159	0.0271	0.0271	0.0182	0.0162	0.0162	0.0278	0.0278
delta[%]	3.44	3.56	3.56	4.08	4.08	2.56	2.12	2.12	3.61	3.61	2.43	2.16	2.16	3.71	3.71
Corner		typ_hh	typ_hl	typ_lh	typ_ll		typ_hh	typ_hl	typ_lh	typ_ll		typ_hh	typ_hl	typ_lh	typ_ll
min. [V]		0.7356	0.7356	0.7488	0.7488		0.7408	0.7408	0.7483	0.7483		0.7384	0.7384	0.7484	0.7484
max. [V]		0.7622	0.7622	0.7763	0.7763		0.7565	0.7565	0.7735	0.7735		0.7542	0.7542	0.7747	0.7747
delta [V]		0.0266	0.0266	0.0275	0.0275		0.0157	0.0157	0.0252	0.0252		0.0158	0.0158	0.0263	0.0263
delta[%]		3.55	3.55	3.67	3.67		2.09	2.09	3.36	3.36		2.11	2.11	3.51	3.51

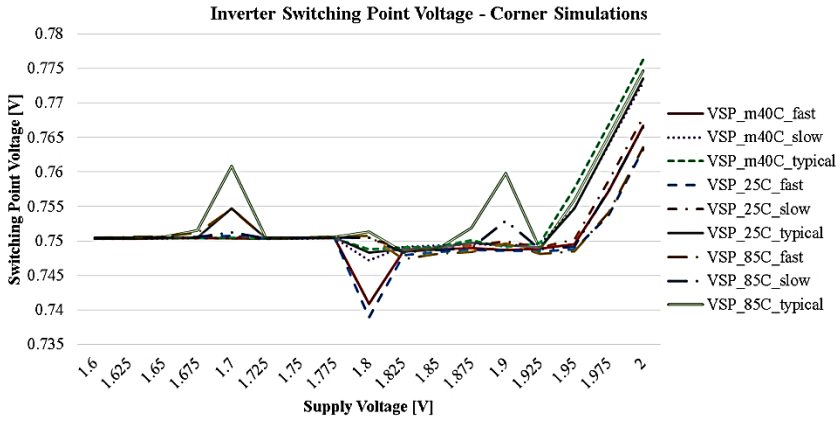

Fig. 12 Inverter switching point – Technological corners simulation results

4. CONCLUSIONS

The present work proposes a compensation technique for the inverter switching point supply voltage variation. This is based on bulk voltage regulation and variable inverter geometry.

The circuit has a maximum power supply switching point variation of 4% (simulated in technological corners, complete with temperature variation). This represents the difference between the maximum and minimum V_{SP} values, and it is computed using the 0.75V switching point (at 1.8V supply voltage) value as reference.

Compared to the original inverter (simulated in the nominal corner at 25ºC), the compensation scheme brings an improvement of 16% for V_{SP} variation (or a 5 times lower variation).

The compensation technique implies nodal capacitance variation according to circuit operation and supply voltage variation. For this reason, there is the need to take precautions when using the proposed circuit for generating time delays.

An oscillator circuit is a typical application for the proposed circuit. Schematic is proposed in [9].

The additional circuitry, for bulk voltage regulation and transistor switching, brings both additional area and power consumption. For the typical application presented in [9], the frequency accuracy increased almost 6 times for, at most, 20% higher power consumption.

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