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TOPOLOGY, ANALYSIS, AND CMOS IMPLEMENTATION OF SWITCHED-CAPACITOR DC-DC CONVERTERS

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Abstract. *This review highlights various design and realization aspects of three commonly used charge pump topologies, namely, the linear, exponential, and the Fibonacci type of charge pumps. We shall outline the new methods developed recently for analyzing the steady and dynamic performances of these circuits. Some practical issues for the CMOS implementation of these charge pump structures will be critically discussed. Finally, some conventional voltage regulation methods for maintaining a stable output under a large range of loading current and supply voltage fluctuations will be proposed.*

Key words: *Switched-capacitor DC-DC converters, charge pump, steady-state analysis, dynamic analysis, voltage regulation*

1. INTRODUCTION

Switched-capacitor DC-DC converter (or SC DC-DC converter, in short) is a kind of voltage converters which realizes a DC-to-DC voltage conversion using capacitors as the only energy storage elements. Unlike the conventional inductor-based DC-DC converters, no inductor is used in the SC DC-DC converters and that makes this kind of converter to have less EMI emission, more compact in size, and is easier for system integration. When compare with the low-dropout regulators (LDO) which can provide step-down conversion only, the SC DC-DC converters have the advantage of being able to generate a voltage higher than the supply. However, the conversion efficiency of a SC DC-DC converter is usually poorer than those of inductor-based converters and the silicon area occupation of a SC DC-DC converter is much larger than that of a LDO. Nevertheless, SC DC-DC converters have been widely used for voltage generation in flash memory systems [1]-[3] and LCD driver circuits where DC voltages higher than the supply voltages are required [4], [5]. SC DC-DC converters are also used in energy harvesting system, self-powered systems like biomedical implant devices, RFID, and wireless sensor networks [6]-[11] where the available source voltages are too low to be used for operating any electronic

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devices. The step-up capability and the ease of CMOS implementation feature of the SC converters can also help to minimization the power consumption of some electronic systems [12], [13].

A SC DC-DC converter consists of an output capacitor (capacitor which is connected across the output node and the ground) and some coupling capacitors which are connected to different nodes in the circuit during the two system clock phases through some power switches. (There are some other structures using more than two clock signals. These structures are more complex and the analysis will be much more complicated. In this work, we shall focus on the two-phase configuration only.) After the clock signals being applied, the coupling capacitors in the converter will be charged and discharged alternately during the charging and discharging phases. During these processes, the energy is temporarily stored in the coupling capacitors and then transferred to other capacitors via the charge sharing nodes. In this way, the energy can be transferred from the input side to the output side via the coupling capacitors, and a desired power conversion can be achieved.

The output voltage of a SC DC-DC converter is governed by its switch-capacitor network or the basic topology. Higher conversion ratio, defined as the ideal output voltage divided by the supply voltage, can be achieved by cascading several units of the basic topology. In this paper, we shall first review some commonly used topologies in Section 2. Because of the charge sharing effects, the switching loss due to the finite "on"-resistance of the CMOS switches, the performances of a SC converter are always poorer than the ideal ones. With these connections, we shall look at some circuit analysis methods that took the non-ideal conditions into consideration. We shall compare the performances of various SC converters using these methods. These ideas together with some typical results will be presented in Section 3. On the other hand, process requirements for CMOS realization of the different SC DC-DC converter topologies will also be different. The practical issues for the CMOS implementation will also be discussed in Section 4. Finally, the implementations of the voltage regulating building block, i.e., the output stage of the converter, will be discussed briefly in Section 5.

2. SC DC-DC CONVERTER TOPOLOGIES

A SC DC-DC converter can be constructed with several different topologies. Different conversion ratios can be achieved by cascading different numbers of stage n. The linear, Fibonacci and exponential topologies, shown respectively in Fig. 1, 2 and 3, are the most commonly used topologies for stepping up a supply voltage [14]-[16]. For the linear topology shown in Fig. 1 [14], which is also known as the Dickson charge pump, the voltage across the coupling capacitor in each stage is stepped up by a value equal to the supply voltage, V_{DD}, during the clock phase Φ_1 or Φ_2. Therefore, by cascading n repeating units, an output voltage equal to $(n+1)V_{DD}$ can be achieved in ideal case, i.e. the conversion ratio M is equal to $(n+1)$. For the Fibonacci topology in Fig. 2 [15], the coupling capacitor in the k-th stage is charged to $F(k+1)V_{DD}$ in Φ_1 and Φ_2 for odd and even k values, respectively. Here $F(x)$ is the x-th member in the Fibonacci series defined by 1, 1, 2, 3, 5, 8, 13, 21, ⋯. The conversion ratio of an n-stage Fibonacci converter is given by $F(n+2)$. For the exponential topology given in Fig. 3 [16], the step-up voltage at the output of each stage will become the input voltage of next stage. Hence the conversion ratio of an n-stage exponential converter is given by 2^nV_{DD}. Comparing these three converter topologies, the

Fibonacci and the exponential topologies can achieve a higher conversion ratio with smaller number of stage and thus fewer components for implementations; whereas the linear topology has the advantage of the smaller voltage stress across the switches. Note that the aforementioned topologies are not limited to step-up operation. By considering the input and output nodes of the step-up converter topologies as the output and input nodes, step-down operation is also possible. In the step down operation, the corresponding conversion ratios for the linear, Fibonacci and the exponential topologies are, respectively, $1/(n+1)$, $1/F(n+2)$ and $1/2^n$.

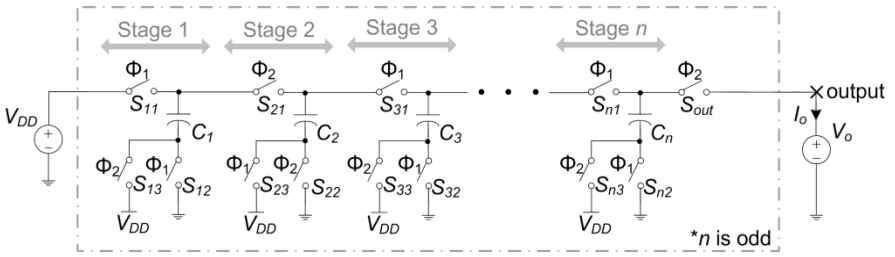

Fig. 1 Topology of a Dickson charge pump or the linear step-up SC DC-DC converter

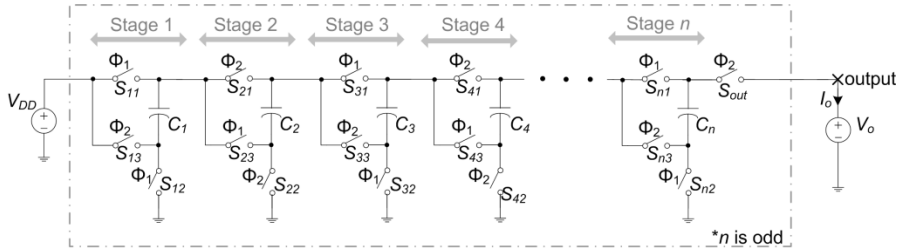

Fig. 2 Topology of a Fibonacci step-up SC DC-DC converter

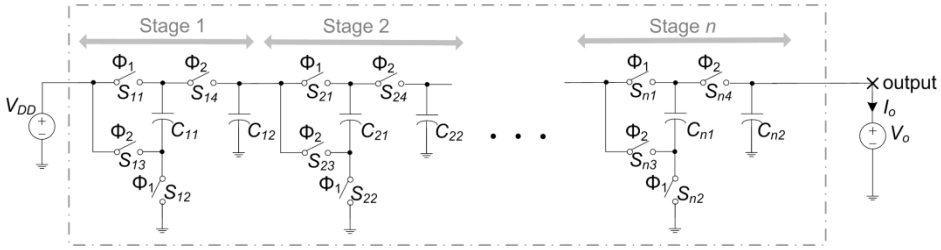

Fig. 3 An exponential step-up SC DC-DC converter topology

3. Performance Analysis

For a practical SC DC-DC converter, its performances vary with different design parameters and are different from the ideal ones. The major design parameters including the number of stage (n), the supply voltage (V_{DD}), the operation frequency (f), the unit value of the coupling capacitance (C), the "on"-resistance (R_{on}), the clock duty cycle (D),

the output capacitance (C_o), and the top- and bottom- plate parasitic factors (α and β), which are defined as the ratio of the parasitic capacitances at the top- and bottom- plates of a capacitor to the capacitance value. The mathematical relationships between these parameters and the performances of the converters have been analyzed in many previous publications. This section highlights these results.

3.1. Output voltage

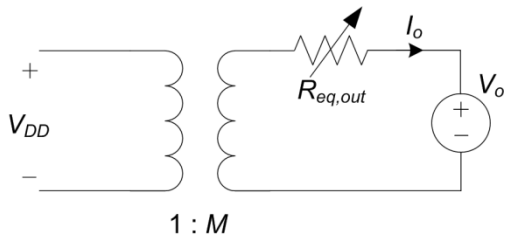

Fig. 4 Equivalent circuit of a SC DC-DC converter [19]

The output voltage of a SC DC-DC converter (V_o) is always smaller than the ideal one as suggested by the conversion ratio M and it depends on the loading current I_o also. This behavior can be modelled by taking an equivalent output resistance into consideration (see Fig. 4). The value of the resistance depends on the charging status or operation mode of the converter [17]-[20]. The charging status can be modelled with $\psi = 1/(2fCR_{on})$ [17], [18], [20]. When $\psi > 1$, the converter is operated in the complete charge transfer mode. The charge transfer among the capacitors in the converter is complete that the current in each path of the converter drops closed to zero at the end of each clock phase. The equivalent output resistance of the converter mainly depends on the $1/(fC)$ factor. When $\psi < 1$, the converter operates in the non-complete charge transfer mode. The charge transfer among the capacitors in the converter is far from complete that the current in each path of the converter is almost constant during each clock phase. The equivalent output resistance of the converter mainly depends on R_{on}. When $\psi \approx 1$, the converter operates between the non-complete and the complete charge transfer mode, i.e. partially charge transfer mode, in which the equivalent output resistance of the converter depends on both $1/(fC)$ and R_{on}. The equivalent output resistances of the converter operated at the slow switching limit (SSL), for which ψ is closed to infinitive; or at the fast switching limit (FSL), for which ψ is closed to zero, theoretically. Models for the equivalent output resistances of the Dickson charge pump at the SSL [21]-[25] and FSL [26], [27] are often reported. It was also suggested that the variation on the equivalent output resistance of the Dickson charge pump across different operation modes can be modeled by the $\coth(x)$ function [28], [29]. The equivalent output resistances of the Dickson and the Fibonacci converters at the SSL, with the consideration of the parasitic capacitance factors, are compared in Ref. [30]. A generalized method for finding the equivalent output resistances of different converter topologies at the SSL and FSL has been proposed [19]. For SSL case, the equivalent output resistance of a given converter can be approximated by [19]:

$$R_{SSL} = \sum_k \frac{(a_k)^2}{fC_k}, \tag{1}$$

where a_k is the charge multiplier of the k-th capacitor C_k. The parameter models the amount of charge flow into the component and is normalized by the amount of output flowing charge. For FSL case, the equivalent output resistance of a given converter topology can be approximated by [19]:

$$R_{FSL} = 2\sum_{k}(a_k)^2 R_{on,k}, \tag{2}$$

where $R_{on,k}$ is the "on"-resistance of the k-th switch and a_k is the corresponding charge multiplier.

3.2. Power efficiency

Power efficiency is an import figure of merit of the Dickson charge pump and is often analyzed or modelled by taking the parasitic losses into consideration. Without considering the parasitic capacitances, finite switch "on"-resistances, and the switching losses for the gate-capacitances of the power switches and the clock drivers, the power efficiency of a converter can be simply determined by $V_o/(MV_{DD})$ [31]. Considering the switching losses of the parasitic capacitances, more accurate solutions were developed [21], [22], [32]. The power efficiency of some practical converters in terms of transistor parameters can also be found [33]. This model took the parasitic resistances, gate capacitances and the top- and bottom- plate parasitic factors into consideration. In general, the power efficiency is given by:

$$\eta_{eff} = \frac{P_{out}}{P_{out} + P_{R,eq} + P_{dyn}} \times 100\%, \tag{3}$$

where P_{out} is the output power, $P_{R,eq}$ is the power loss of the equivalent output resistance and P_{dyn} is the total switching loss due to gate capacitances, top- and bottom- plate parasitic capacitances, and the clock driver. Thus, $P_{R,eq}$ increases with the equivalent output resistance; and P_{dyn} increases with the parasitic factors, α and β, clock frequency, supply voltage, and the size of the power switches. The increment of both P_{dyn} and $P_{R,eq}$ gives rise to a lower power efficiency. Notice that the power efficiency of a converter varies with the loading current, and the maximum achievable power efficiency of a given design can only be determined with a given value of loading current and output voltage. By assuming that the conversion ratio and the equivalent output resistance are independent of the parasitic factors, the condition for maximum power efficiency can be determined accordingly [34]. It was found that as the parasitic factors increase, the maximum power efficiency occurs at a large loading current.

3.3. Output voltage ripple

The behavior of output voltage ripple in a SC DC-DC converter can be understood as follow. Let us consider a converter, see Figs. 1 to 3 for example, has an output capacitor C_o and its loading current be I_o. As the output capacitor is not charged by the converter during Φ_1, the loading current is governed by the charge stored in the output capacitor only. Hence the output voltage would have the smallest value of ripple of $I_o/(2fC_o)$ when D =0.5. The largest value of the ripple is $I_o/(fC_o)$ when the total amount of charge equal to I_o/f. This occurs when the charge consumed by the load in a single clock cycle is transferred instantaneously to the output capacitor at the beginning of Φ_2 in each clock cycle. Hence,

when a converter is operated in the complete charge transfer mode, its output voltage ripple is more likely to be larger than the minimum value. On the other hand, the output voltage ripple is closed to the minimum value when the converter is operated in the non-complete charge transfer mode. A detailed discussion on the output voltage ripple under different operation modes can be found in Ref. [20].

3.4. Start-up time

If the capacitors in Fig. 1, 2 and 3 are not charged at the beginning, it takes several clock cycles for the coupling capacitors to transfer charge to the output C_o. That is, a converter will take certain time to reach its steady output voltage. This time interval for this transient period is known as the start-up time. During this period, the charge flowing in and out of the capacitors are not the same for some clock cycles. Finding the start-up time requires some dynamic analyses of the converter. With the aid of dynamic analyses, closed-form solutions for the start-up times of some linear converters with different numbers of stage and parasitic factors were obtained [34]-[40]. A generalized method which can evaluate the start-up behaviors of any forms of converter topologies was proposed [41]. It involves the

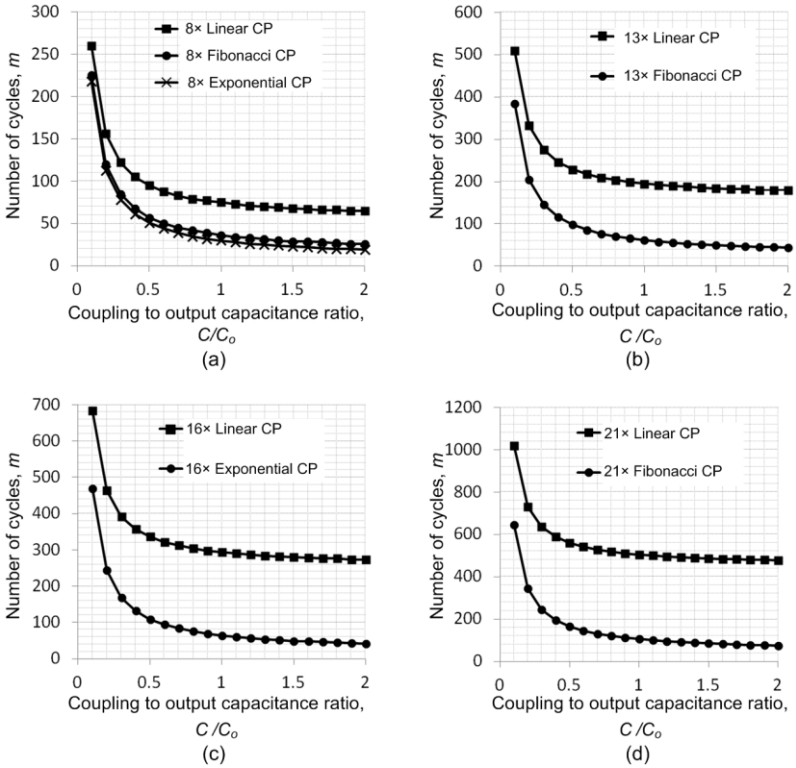

Fig. 5 Plots of the required number of clock cycles for achieving 95% of final values for linear, Fibonacci and the exponential converters as a function of coupling-to-output capacitance ratio for the case of the conversion ratio equal to: (a) 8; (b) 13; (c) 16; and (d) 21 [41]

formulation of a given converter topology into some matrices, from which the output voltage of a converter can be evaluated with time using the matrix equations. In the analyses, we assume: (a) the converter is operated at SSL mode with capacitive loads only; (b) all the capacitors in the converter are initially uncharged; (c) the parasitic capacitance effects can be neglected. Based on these assumptions, the number of cycle, *m*, for achieving 95% of final output value can be determined. Figure 5 plots the number of cycle as a function of coupling-to-output capacitance ratio (defined by C_o/C) for the case of n=8, 13, 16 and 21[41]. It can be found that for a converter to have a short start-up time, the output capacitance should not be larger than 2 times of the coupling capacitance.

3.5. Performance comparison of different topologies

This section concludes with the performance comparison as given in Table 1. Table 1 lists the performances of the 8× linear, Fibonacci and exponential converter with same conversion ratio. Note that the equivalent output resistance of the linear converter at the FSL mode is smaller than those of the Fibonacci and the exponential ones. In addition, the voltage stress across the transistors in the linear converter is smaller regardless the large number of cascading stages. However, the linear converter requires larger number of components to implement and has a longer start-up time. Further detailed comparison on the performances of these kinds of converters can be found in Refs. [42], [43].

Table 1 Comparison of the linear, Fibonacci and exponential topologies with M = 8

Topology	n	No. of switch	No. of capacitor	Max. blocking voltage (V)	$R_{eq,out}$ SSL ($1/(Cf)$)	$R_{eq,out}$ FSL (R_{on})	Start-up time (no. of clock cycle, m, for C/C_o=1)
Linear	7	22	7	$2V_{DD}$	7	44	75
Fibonacci	4	13	4	$5V_{DD}$	7	52	36
Exponential	3	12	5	$4V_{DD}$	10	56	30

4. CMOS Implementation of SC DC-DC Converters

The SC DC-DC converter topologies given in Section 2 can be implemented using the standard CMOS technology by realizing the switches with some N-type or P-type CMOS switches (or called the CTS's). To minimize the reverse current and the output voltage drop, these switches should be biased in the cut-off region and the triode region when they are turned off and on, respectively. The reverse current can be further reduced by applying non-overlapping clock signals [44]. The body effects, i.e. the non-zero source-to-bulk biasing voltages, in these switches can lead to a larger threshold voltages and make the output voltage be saturated at a lower value [45]. Hence, for a step-up SC DC-DC converter, we may encounter some unexpected voltage drop and power losses. In addition, as the node voltages in a step-up SC DC-DC converter are higher than V_{DD}, several factors need to be considered. Here lists some issues need to be take care:

- In the step-up voltage converters, the node voltages (and therefore the drain and the source voltages of the transistors) are higher than V_{DD}. Thus, a P-type CTS can be turned on easily by applying 0V (or any voltage lower than its source/drain voltage by a threshold) at the gate. However, a gate voltage higher than V_{DD} is usually required to shut down the CTS completely, which may not be available in the circuit. On the other hand,

an N-type CTS can be readily shut down by applying 0V (or any voltage lower than its source/drain voltage plus a threshold) at the gate. However, to turn on the CTS completely, the gate voltage should be higher than V_{DD}. The bodies (or the N-wells if the converter is implemented in an ordinary N-well process) of the P-type CTS's are usually required to be biased at a voltage higher than V_{DD} such that the P-N junctions in the transistors can be always in reversely biased. Otherwise, substrate leakage current exists and the converter would have poor efficiency. On the other hand, if the bodies of the N-type CTS's are biased at 0V (which is the usual case for the circuits implemented in an ordinary N-well process), they will suffer from the body effect and that the threshold voltages of the CTS's will become larger. As the node voltages in the linear topology increase linearly from the input side to the output, while those in the other ones can rise exponentially. Thus, it is easier to design an efficient converter using the linear topology.

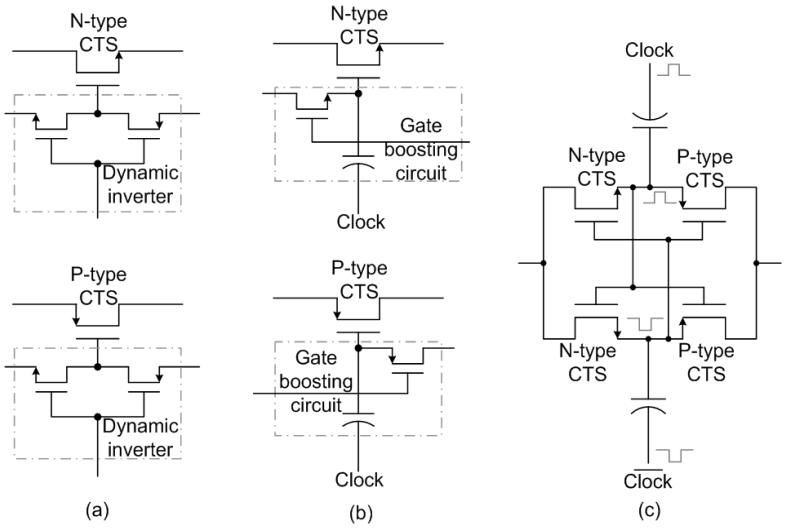

Fig. 6 Illustration of the three gate-biasing techniques: (a) the dynamic biasing; (b) gate-boosting; and (c) the cross-coupled techniques [46]-[49]

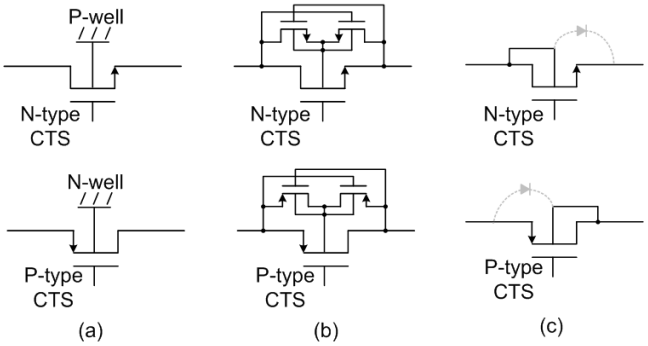

Fig. 7 Illustration of the three body-biasing approaches: the (a) floating-well; (b) adaptive body-biasing; and the (c) body-source junction diode approaches [50]-[52]

- In the step-down voltage converters, the node voltages (and therefore the drain and the source voltages of the transistors) are between 0V and V_{DD}. Thus, the body and the gate terminals of both N- and P-type CTS's can be biased properly without any difficulties. However, the use of N-type CTS can usually save more silicon area due to its higher transconductance. To pass a voltage in the range of 0V to V_{DD}, transmission gates can be used.

To achieve higher power efficiency, several different gate- and body- basing techniques have been proposed to control the CTS's in the Dickson charge pump. Figure 6 shows the dynamic biasing [46], gate boosting [47], [48] and the cross-coupled techniques [49] for gate biasing. Figure 7 shows some techniques including the floating-well [50], adaptive body-biasing [51], and the body-source junction diode approach [52], to alleviate the body effects of the CTS. The advantages and disadvantages of these techniques have been discussed in detail in Ref. [53]. In short, small output voltage drops can be found in the converters using the gate boosting and the cross-coupled techniques, but the gate-boosting technique would consume larger dynamic power and the cross-coupled technique requires a costive triple-well process. Advanced converter circuits are usually constructed by making use of more than one of these techniques [54], [55].

Figures 8 and 9 present the measurement, simulation, as well as the theoretical results on the loading characteristics and the power efficiencies of the CMOS 4× exponential converter at four different frequencies ranging from 25 kHz to 200 kHz [56], [57]. All the switches in this converter are turned on and off properly with additional dynamic inverters. The circuits were designed for operation at V_{DD} = 1.5V, C = 100 nF, and assuming R_{on} of the

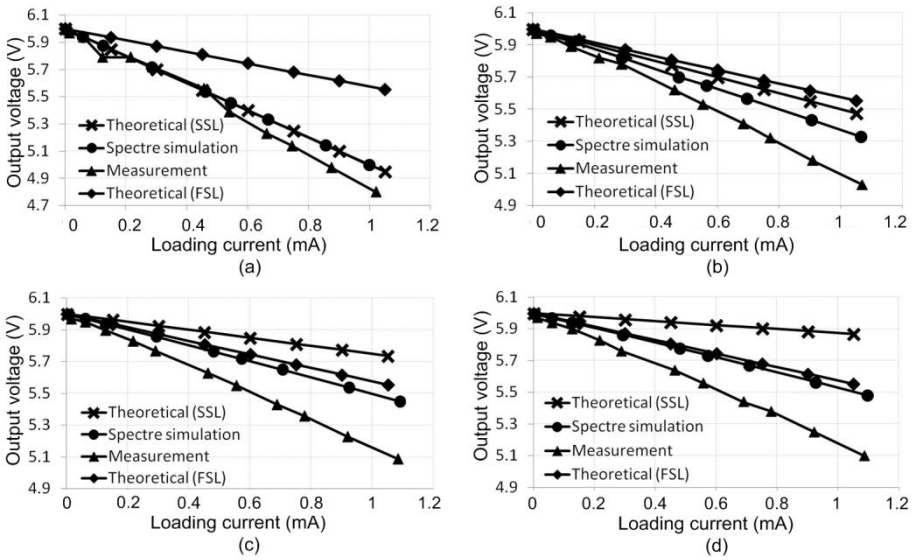

Fig. 8 Theoretical (both the SSL and FSL cases), simulated, and measured loading characteristics of the 4× CMOS exponential converter proposed in Ref. [57] with V_{DD} = 1.5V, at four different frequencies: (a) 25 kHz; (b) 50 kHz; (c) 100 kHz; and (d) 200kHz

switches be 50 Ω. For f = 25 kHz, 50 kHz, 100 kHz and 200 kHz, the corresponding ψ values are equal to 4, 2, 1 and 0.5, respectively. Thus, it is expected that the designed converter is more likely to be operated at the SSL mode with $R_{eq,out}$ given by eq. (1) for f = 25 kHz and 50 kHz. For f = 100 kHz and 200 kHz, they are at FSL mode and $R_{eq,out}$ is given by eq. (2). The simulation results shown in Fig. 8 agree well with this conjecture. In Fig. 8, loading characteristics are more or less the same. It further prove that the designed circuit should work at the FSL when f = 100 kHz and 200 kHz. It is because the equivalent output resistance of a converter at FSL should be independent of the operation frequency according to eq. (2). The difference between the theoretical and the measurement results in Fig. 8(a)-(d) should be due to the equivalent series resistance (ESR) of the externally connected capacitors, interconnections, and the parasitic capacitances at each node of the real circuit. This difference is less than 10% [57]. In Fig. 9, it can be further observed that when the frequency is increased from 25 kHz to 200 kHz, the measured power efficiency drops from 80% to 40% when the loading current is small. This agrees well with what suggested by eq. (3). In eq. (3), the dynamic power loss, P_{dyn}, dominates when the output power is small, and P_{dyn} increases with the operation frequency [57].

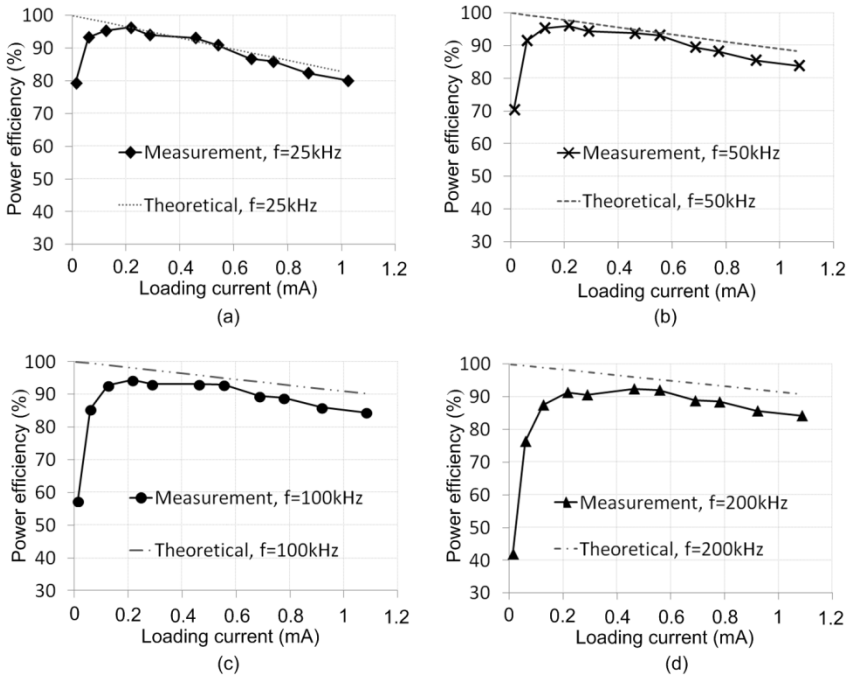

Fig. 9 Theoretical and measured power efficiencies versus loading current of the 4× CMOS exponential converter proposed in Ref. [57] with V_{DD} = 1.5 V, at four different frequencies: (a) 25 kHz; (b) 50 kHz; (c) 100 kHz; and (d) 200 kHz

5. REGULATIONS IN SC DC-DC CONVERTERS

As shown in Fig. 8, the output voltages of the SC DC-DC converters drop as the loading currents increase. To maintain a constant output voltage under different loads, a better regulation method that using a closed-loop structure is required for the SC DC-DC converters. On the other hand, the supply voltage, like the battery used in some portable devices, may also drop significantly during the operation and that causes the output voltage of the DC-DC converters to drop continuously as the output voltage of a SC DC-DC converter is directly proportional to the supply voltage. Hence, we need to maintain the output voltage over a wide supply voltage range also. These are the main tasks for the output stage of the converters. In this section, a review on some previously proposed regulation techniques will be given.

5.1. Regulation for loading current fluctuation

Pulse-skipping modulation (PSM) technique was found to be well suit for SC DC-DC converter applications. Fig.10 illustrates the schematic of this this method. By skipping some of the charge transferring periods for the output according to the loading condition, a better regulation can be achieved. As shown in the figure, when the loading current decreases, the sensed output voltage, V_{fb}, may become larger than that of the reference one, V_{ref}, the clock signals for controlling the converter will be shut down. The converter will then be disconnected from the output in effect and that stops further delivering power to the output. When V_{fb} drops below V_{ref} due to the discharging loading current, the output capacitor will be recharged by the converter again. By this way, the charge transferring period for the output (or the average power delivering to output) can be adjusted such that constant V_o will be kept under different I_o. Here a hysteresis comparator is used and ripples exist. This method has the advantages of fast response and good stability. Moreover, the switching loss can be reduced and the power efficiency can be improved especially when I_o is small. However, variable operation frequency and large output voltage ripple, are the main drawbacks of this method [58].

Alternatively, as illustrated in Fig. 11, the output voltage can be regulated by adjusting the coupling capacitors charging current according to the loading condition. In this linear control method, some transistors are used as voltage-controlled current sources and are included in the charging paths of the converter. The error amplifier in the negative feedback loop then controls the current sources, and thus the charging currents to the coupling capacitors according to the loading condition. Unlike the PSM method, this control method produces smaller output voltage ripple and makes use of invariant operation frequency. Unfortunately, the switching loss is comparatively large when the loading current is small and that leads to poorer power efficiency [31], [59].

Other regulation methods proposed in the literatures frequency modulation, segmented output components [60]-[65]. In the frequency modulation method, the output is regulated by adjusting the operation frequency of the converter. It uses a voltage-controlled oscillator (VCO) in the feedback loop [60], [61]. As the equivalent output resistance of a converter is related to the component sizing (see eq. (1) and (2)), the output voltage of a SC DC-DC converter can also be regulated using some segmented devices, like the segmented capacitors [62], [63] and the segmented CTS's [64], [65]. Regulated converters using more than one of the above techniques can also be found in some reports. For example, Bayer and Schmeller [66] used both the linear control and the PSM methods to regulate its output

voltage. Patounakis, Li and Shepard proposed a hybrid regulator that combines the SC DC-DC converter and the low dropout regulator (LDO) to achieve high efficiency and to reduce the voltage ripple [67].

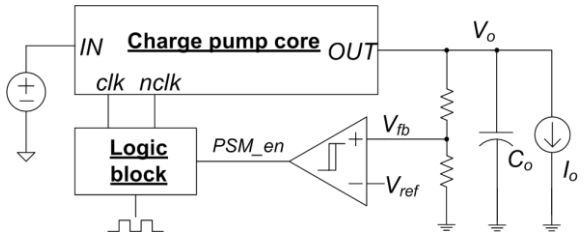

Fig. 10 Illustration of the pulse-skipping modulation method used for charge pump voltage regulation

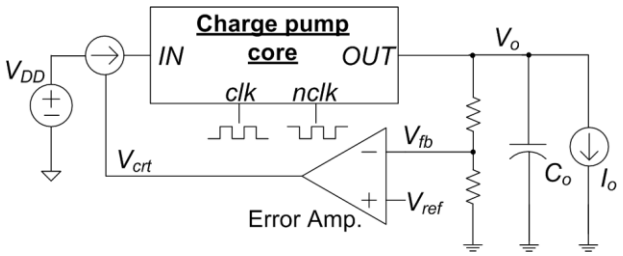

Fig. 11 Illustration of the linear control method used for charge pump voltage regulation

5.2. Regulation on supply voltage variation

As mentioned, SC DC-DC converters are often used in systems with varying supply voltage. It was realized that regulating a SC DC-DC converter over a wide supply voltage range based on simple feedback loops, like the ones shown in Fig. 10 and 11, often results in a poor power efficiency as the maximum achievable power efficiency of a SC DC-DC converter is given by $V_o/(MV_{DD})$. Hence, to maintain a certain output voltage, the power efficiency will drop with the supply voltage if the switch-and-capacitor-network configuration is not altered (.i.e. M is fixed). With this connection, reconfigurable SC DC-DC converters, in which the switch-and-capacitor-network configuration could be alterable, i.e. M is an available, were proposed. This method improves the power efficiency over a wide range of supply voltage. This idea can be demonstrated by considering the case that a fixed output voltage of 1.8V is required and the supply voltage may vary in the range of 3-5 V. In this case, the theoretical maximum power efficiencies which can be achieved by some SC DC-DC converters with different available M values under different supply voltages are plotted in Fig. 12. Clearly, higher overall power efficiency can be achieved with a converter having more available conversion ratios. Fig. 13 illustrates the control of the reconfigurable SC DC-DC converter. Additional circuitries are added to determine the M value of the converter based on the V_{DD} value. That minimizes the dropout voltage at different supply voltages [68]-[71]. More complicated techniques, such as the gain hopping technique [72]-[74], were proposed to determine the M value based on the loading condition also so as to further improve the overall power efficiency.

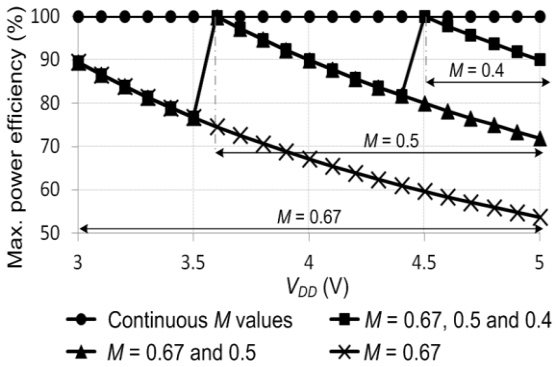

Fig. 12 Plot of the theoretical maximum power efficiencies at different V_{DD} for a reconfigurable converter using different M values for constant V_o of 1.8V

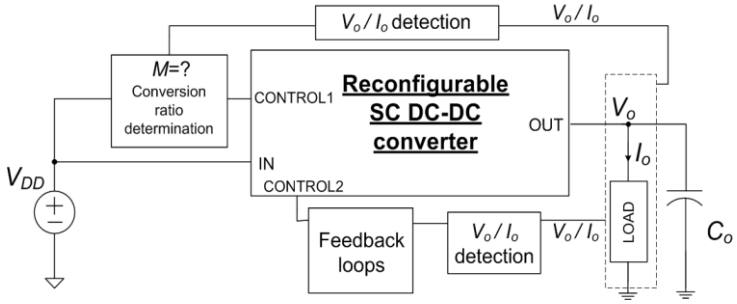

Fig. 13 Illustration of the control of a reconfigurable SC DC-DC converter

6. Conclusion

An overview on two-phase switched capacitor DC-DC converters is given. Characteristics, including equivalent output resistances, power efficiencies, voltage ripples, and start-up times, of three commonly-used topologies, i.e. the linear, Fibonacci, and the exponential topologies, are compared. Some practical issues on the implementation of these converters using CMOS technology are discussed. Finally, revised voltage regulation schemes, being able to accommodate a wider range of loading current fluctuation, are proposed for high-efficiency voltage conversion.

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