A Novel Modeling and Control Design of the Current-Fed Dual Active Bridge Converter under DPDPS Modulation

Phuong Vu
School of Electrical Engineering
Hanoi University of Science and Technology
Hanoi, Vietnam
phuong.vuhoang@hust.edu.vn

Do Tuan Anh
School of Electrical Engineering
Hanoi University of Science and Technology
Hanoi, Vietnam
tuananhdo.hust@gmail.com

Hoang Duc Chinh
School of Electrical Engineering
Hanoi University of Science and Technology
Hanoi, Vietnam
chinh.hoangduc@hust.edu.vn

Abstract-This paper proposes a novel control design for a Current-Fed Dual Active Bridge (CFDAB) converter in boost mode. The Double PWM plus Double Phase Shifted (DPDPS) modulation is applied to the converter due to its considerable merits. A small-signal model is developed to control the output voltage stably in boost mode. Simulations of the control design for the CFDAB converter were conducted to verify the proposed model. The results show that the system can achieve high performance, not only in the dynamic response but also in the steady-state.

Keywords-Current-Fed Dual Active Brigde (CFDAB) converter; small-signal model; Double PWM plus Double Phase Shifted (DPDPS) modulation

I. INTRODUCTION

Nowadays, the growth in renewable power systems urges researchers and engineers to solve the problems of managing integrated storages and exchange powers to enhance overall system efficiency. In order to connect the battery at low voltage to the DC link at high voltage in a storage system, the utilized DC/DC converter needs to have a high gain voltage factor and an ability of bidirectional transferring power. The DC/DC converters can be classified as isolated and non-isolated. Between these two, the isolated DC/DC converter is highly recommended for its high reliability. It is able to eliminate current leakage in the system. This undesired current is the cause of EMI, additional loss, and unsafe installation and operation [1]. Another advantage of the isolated DC/DC converter is that the flexible gain ratio can be obtained by using a high frequency transformer [2, 3]. The Dual Active Bridge (DAB) converter belongs to the isolated DC/DC type and is well-known for its advantages of high frequency operating ability, inherit zero voltage switching, and bidirectional power flow [4-6]. The structure of the DAB can have modified flexibly with different power sources [7-8]. The DAB converter is divided into two categories: Voltage-Fed (VFDAB) and Current-Fed (CFDAB). When using the VFDAB structure in a variety of applications [9-11], the voltage source is directly supplied to the converter, which produces high current ripple and becomes large and costly. Besides, the VFDAB needs a bulky capacitor in series-connection with the primary coil to avoid the flux saturation of the transformer [11]. Therefore, the CFDAB structure is used to deal with these problems, the input interleave boost inductors in CFDAB help to decrease the current ripple significantly, and ZVS can be achieved for all switches over a wide range of load [9-12].

On the other hand, a small-signal model needs to be built for the accurately controlling problem. Naturally clamped CFDAB modeling structure has been introduced in [13, 14]. Besides, a state-space model under SPSPWM modulation for interleaved boost CFDAB structure is mentioned in [15]. In the current research, DPDPS modulation technique in comparison with SPSPWM modulation [9] is applied, and a small-signal model to regulate the output voltage is built up in boost mode. The simulation results show the effectiveness of the proposed method.

II. RESEARCH METHOD

A. Operation Principles and Control Structure

1) Operation Principles

The applied structure of CFDAB converter in this research is presented in Figure 1, which consists of 2 main parts: the interleaved boost part and the dual active full-bridge part. In the interleaved boost part, two DC inductors are considered as two current sources. The inductor L_{dc1} is combined with the left leg containing the switch pair Q_1, Q_{1a} to create the first boost converter, while the right leg containing the Q_2, Q_{2a} switch pair is combined with the inductor L_{dc2} to create the second boost converter. These boost converters are 180° phase-shifted in order to compose an interleaved boost part, in which the boost voltage is kept by the clamp capacitor C_c.

On the other hand, the dual active full-bridge part consists of two H-bridge modules in two sides of an isolated high frequency transformer with the turn ratio of N: 1.

Corresponding author: Phuong Vu

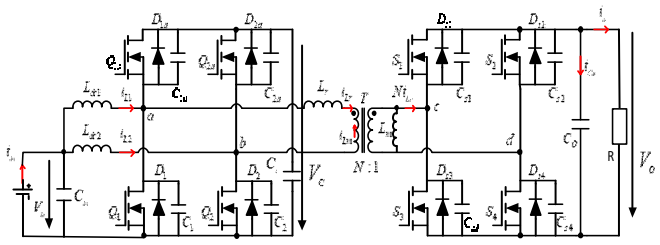

Fig. 1. Structure of the CFDAB converter.

The voltages of the clamp capacitor and the output capacitor are assumed as the Low-Voltage Side (LVS) and High-Voltage Side (HVS). The bidirectional transfer power between the LVS, the HVS, and the power flow are determined by the phase shifted angle. The AC inductor L_r, which is the sum of the primary-referred transformer leakage inductor, which can be considered as a power link between the two sides of the converter.

2) Modulation Strategy

Due to the high amount of switch devices and inductors, the modulation strategy for the converter needs to be considered before designing the control loop. To handle the voltage ratio variation problems and to minimize the conduction loss in power transfer stages, the PWM plus Phase Shifted (PPS) is introduced while the duty cycle for HVS switches is equal to 50% and the duty ratio for the main LVS switches Q_1, Q_2 is a variable D. However, in the non-power transfer stage of PPS, the circulation loss is significant with high leak current spike. An additional phase shifted in Double PWM plus Double Phase Shifted (DPDPS) method [9], which equals to $(2D-1)\times T_s/2$, is applied to eliminate the leak current spike. Figure 2 illustrates the modulation rule of the CFDAB converter, where the phase shifted between Q_1-Q_2, Q_2-S_1 and S_1-S_4 are 180°, φ and φ_S respectively. The value of φ_E determines the power flow and direction, where $\varphi_E>0$ represents the operation boost mode with power flow from LVS to HVS and vice versa. By utilizing DPDPS modulation, 8 operation modes in one switching period along with leakage current, the switching LVS voltage and the transformer voltage waveform v_{cd} are displayed in Figure 3 [9].

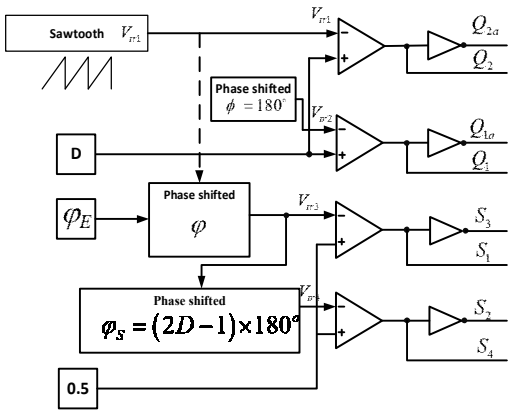

Fig. 2. DPDPS modulation technique for the CFDAB converter.

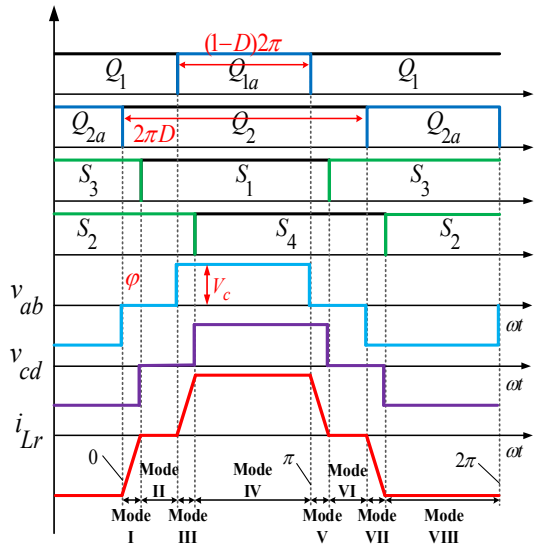

Fig. 3. Pulse patterns, transformer voltage, and leakage current waveforms.

3) Control Structure

For CFDAB converter structure, the transfer power is related to the clamp voltage V_c and the phase shifted φ_E between the two H-bridges. Therefore, the control structure in boost mode has to control the voltage of the clamp capacitor and the output capacitor simultaneously. There are two pairs of control variables: V_c-d and $V_o-\varphi$, as presented in Figure 4.

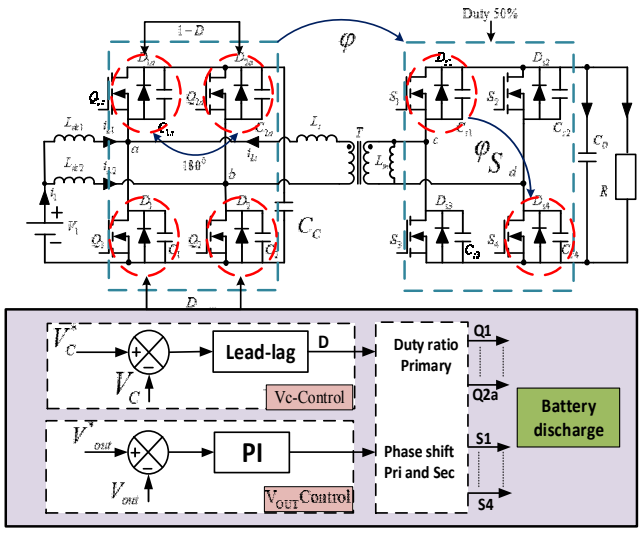

Fig. 4. Control structure in boost mode.

B. Small Signal Modeling

It is required to determine the transfer functions of the two pairs of control variables mentioned above so that the control scheme in Figure 4 can be implemented. The transfer function perturbations between clamp voltage $\hat{v}_c$ and duty ratio $\hat{d}$ is depicted in (1) [9]:

$$G_{v_c\_d} = \frac{\hat{v}_c}{\hat{d}} = \frac{2V_c\varphi - \omega L_r\left(I_{L1}+I_{L2}\right)}{\omega L_r C_d s + 2\varphi(1-D) - \frac{\varphi^2}{2\pi}} \quad (1)$$

In this paper, the small signal model along with the closed loop controller is proposed to regulate the output voltage of the converter under DPDPS modulation. In the secondary side, the output capacitor is charged and discharged in power transfer and non-power transfer stage respectively. From the switching sequence in Figure 3, the time interval of each switching mode is given by:

$$\begin{cases} d_1 = d_3 = d_5 = d_7 = \dfrac{\varphi}{2\pi} \\ d_4 = d_8 = 1-d, \\ d_2 = d_6 = \dfrac{2d-1}{2} - \dfrac{\varphi}{2\pi} \end{cases} \quad (2)$$

The relationship between small signals of variables is presented in Table I for 8 modes in one DPDPS switching period. The inductors and capacitors are considered as ideal, i.e. the internal resistors are neglected. The continuous-time equation of output voltage is defined as:

$$\begin{aligned} C_o\frac{dv_o}{dt} &= N\left(d_4-d_8\right)\frac{\langle v_c\rangle}{\omega L_r}\varphi \\ &+\left(-d_1+d_2+d_3-d_4-d_5+d_6+d_7-d_8\right)\frac{v_o}{R} \\ &+Nd_5\frac{\langle v_c\rangle}{\omega L_r}\left(\pi-\theta_5+\varphi\right)-Nd_1\frac{\langle v_c\rangle}{\omega L_r}\left(\theta_1-\varphi\right) \end{aligned} \quad (3)$$

Using the average model:

$$\theta_7 = 2d\pi + \frac{\varphi}{2}, \langle v_c\rangle = v_c, \theta_3 = (2d-1)\pi + \frac{\varphi}{2}$$

we can obtain:

$$\begin{aligned} C_0\frac{dv_0}{dt} &= N\left(d_4+d_8\right)\frac{\langle v_c\rangle}{\omega L_r}\varphi + N\left(d_1+d_5\right)\frac{\langle v_c\rangle}{\omega L_r}\frac{\varphi}{2} \\ &+\left(-d_1+d_2+d_3-d_4-d_5+d_6+d_7-d_8\right)\frac{v_0}{R} \end{aligned} \quad (4)$$

Replacing (2) to (4) we get:

$$C_0\frac{dv_0}{dt} = \left(4d-3\right)\frac{v_0}{R} + N\left(\frac{-\varphi^2}{2\pi} + 2\varphi(1-d)\right)\frac{v_c}{\omega L_r} \quad (5)$$

Using the perturbations of duty ratio, phase-shifted angle output voltage, and clamp voltage we have:

$$\begin{aligned} C_0\frac{d(V_o+\hat{v}_o)}{dt} &= \left(4(D+\hat{d})-3\right)\frac{(V_o+\hat{v}_0)}{R} + \\ &+N\left(\frac{-(\Phi+\hat{\varphi})^2}{2\pi} + 2(\Phi+\hat{\varphi})(1-(D+\hat{d})\right)\frac{V_c+\hat{v}_c}{\omega L_r} \end{aligned}$$

Discarding the steady-state value and the second order perturbations and assuming that $\hat{d} = \hat{v}_{Cc} = 0$ we get:

$$C_0\frac{dv_0}{dt} = \left(4d-3\right)\frac{v_0}{R} + N\left(\frac{-\varphi^2}{2\pi} + 2\varphi(1-d)\right)\frac{v_c}{\omega L_r} \quad (7)$$

By Laplace transformation, the transfer function from $\hat{v}_o$ to $\hat{\varphi}$ in the frequency domain can be expressed as:

$$G_{v_o\_\varphi} = \frac{NRV_c(2-2D-\frac{\Phi}{\pi})}{\omega RL_r C_0 s - \omega L_r\left(4D-3\right)} = \frac{A}{Bs+C} \quad (8)$$

TABLE I. SMALL SIGNAL MODEL IN EACH SWITCHING MODE

Mode	Continuous- time equations
Mode I $[0, \varphi]$	$C_0\frac{dv_0}{dt} = -\frac{v_0}{R} - Ni_{Lr}, i_{Lr} = \frac{\langle v_c\rangle_{Ts}}{\omega L_r}(\theta-\varphi)$
Mode II $[\varphi, (2d-1)\pi]$	$C_0\frac{dv_0}{dt} = \frac{v_0}{R}, i_{Lr} = 0$
Mode III $\left[(2d-1)\pi, (2d-1)\pi+\varphi\right]$	$C_0\frac{dv_0}{dt} = \frac{v_0}{R}, i_{Lr} = \frac{\langle v_c\rangle_{Ts}}{\omega L_r}\left[\theta-(2d-1)\pi\right]$
Mode IV $\left[(2d-1)\pi+\varphi, \pi\right]$	$C_0\frac{dv_0}{dt} = -\frac{v_0}{R} + Ni_{Lr}, i_{Lr} = \frac{\langle v_c\rangle_{Ts}}{\omega L_r}\varphi$
Mode V $[\pi, \pi+\varphi]$	$C_0\frac{dv_0}{dt} = -\frac{v_0}{R} + Ni_{Lr}, i_{Lr} = \frac{\langle v_c\rangle_{Ts}}{\omega L_r}(\pi-\theta+\varphi)$
Mode VI $[\pi+\varphi, 2d\pi]$	$C_0\frac{dv_0}{dt} = \frac{v_0}{R}, i_{Lr} = 0$
Mode VII $[2\pi d, 2\pi d+\varphi]$	$C_0\frac{dv_0}{dt} = \frac{v_0}{R}, i_{Lr} = -\frac{\langle v_c\rangle_{Ts}}{\omega L_r}\left[\theta-2d\pi\right]$
Mode VIII $[2\pi d+\varphi, 2\pi]$	$C_0\frac{dv_0}{dt} = -\frac{v_0}{R} - Ni_{Lr}, i_{Lr} = -\frac{\langle v_c\rangle_{Ts}}{\omega L_r}\varphi$

C. Simulation Verification

The control design with the proposed method is firstly verified by simulation in Matlab/Simulink (Figure 5). The specifications of the converter are given in Table II and the transfer function in frequency domain between $\hat{v}_o$ and $\hat{\varphi}$ is turned into:

$$G_{vo\_\varphi} = \frac{\hat{v}_o}{\hat{\varphi}} = \frac{A}{Bs+C} = \frac{1.643\times10^4}{0.3213s+4.7} \quad (9)$$

A PI controller is applied to regulate the output voltage:

$$G_c = K_p(1+\frac{1}{Tis}) \quad (10)$$

where T_i is equal to the pole of $G_{v_o\_\varphi}$: $T_i = \frac{B}{C} = 0.068$.

The output voltage close loop transfer can be written as:

$$G_k = \frac{1}{T_k s+1} \quad (11)$$

with $T_k = \frac{B}{A * K_p}$. By choosing $T_k = 5 * T_s = 10^{-4}$, $Kp = 0.276$.

The simulation scenario consists of 4 steps: the clamp capacitor is charged from 0 to 0.2s, at 0.2s the V_c controller starts and the LVS switches are enabled, at 0.25s the V_o controller starts and in the final step, the load changes suddenly to the nominal value. Figures 6, 7 show the simulation results of clamp and output voltage respectively. As can be observed, in the start-up period, the voltages of the two capacitors are charged and controlled to increase gradually as well as track the reference values with negligible error and no over-shoot.

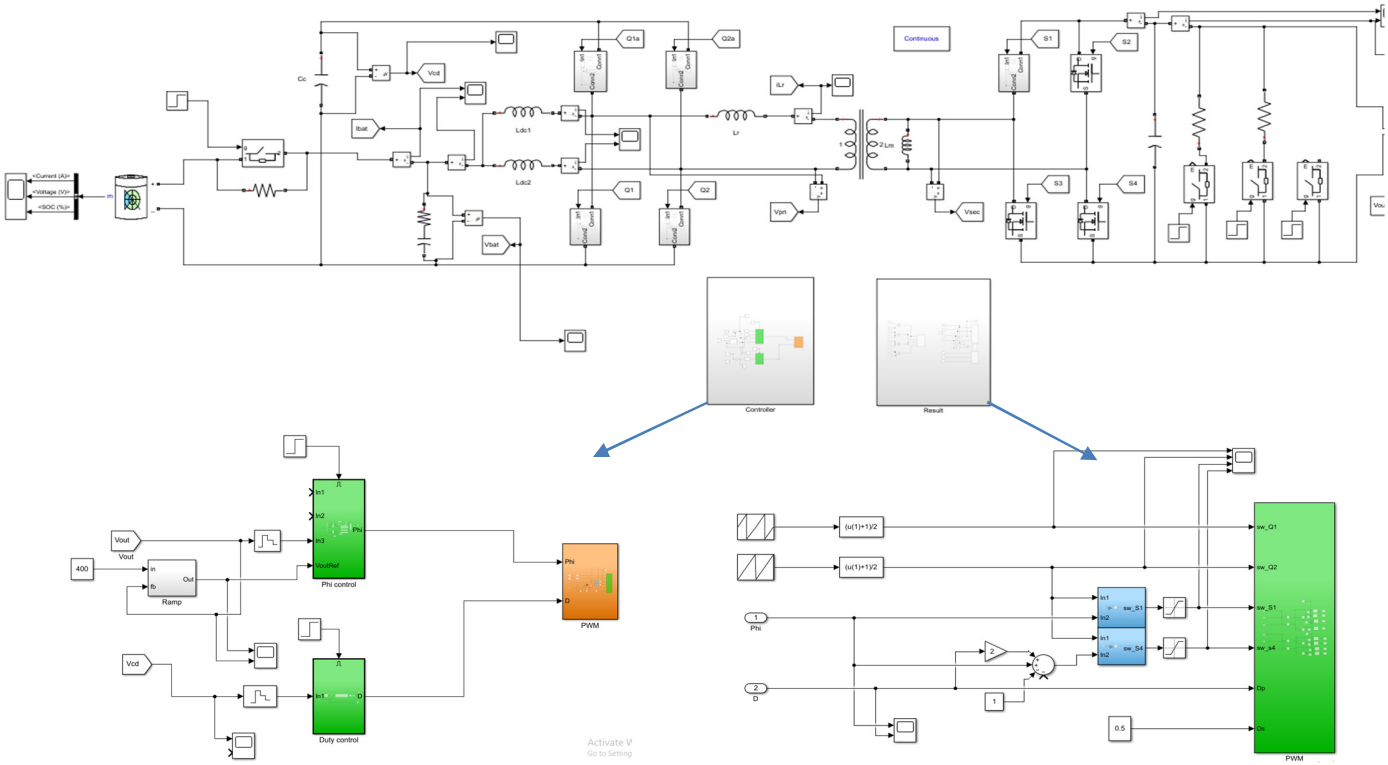

Fig. 5. Simulink model for the control of the CFDAB converter in boost mode.

TABLE II. SIMULATION PARAMETERS

Specification	Symbol	Value
Nominal power	P_n	2500W
Input voltage	V_{in}	144V
Output voltage	V_{out}	400V
Duty ratio	D	0.64
Clamp voltage	V_c	391V
Switching frequency	f_s	50kHz
Nominal duty cycle	D	0.64
Nominal phase-shifted	Φ	0.241

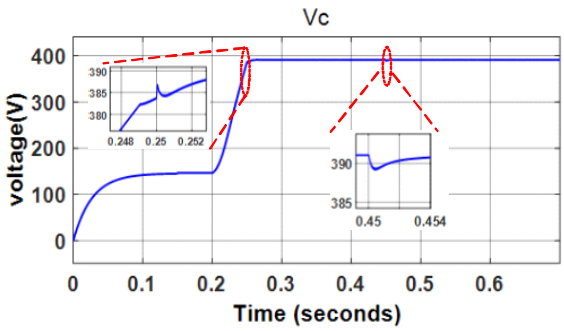

Fig. 6. Voltage response on the clamp capacitor.

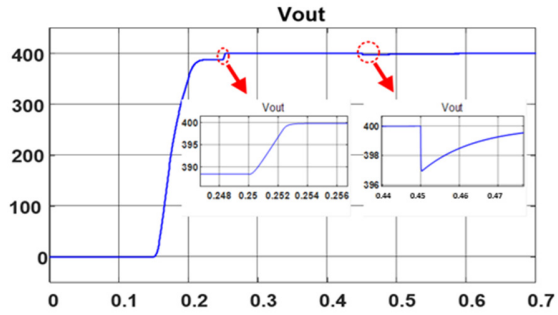

Fig. 7. Voltage response on the output capacitor.

Furthermore, the currents through the boost inductor and the leakage inductor with little spike in the start interval which ensure the feasibility of the control design in the experiment, are shown in Figures 8 and 9. The clamp voltage and the out voltage decrease slightly, about 3V, at 0.45s when the nominal load is changed. After that, they quickly return to the reference value within 0.01s and 0.03s. In steady-state operation, the voltages on both the LVS and HVS side of the transformer along with leakage current are shown in Figure 9. Due to the

small difference between the reference of clamp voltage and the output voltage, the bias current in the leakage current helps HVS switches achieve the ZVS easier [16]. In addition, the switches voltage and current are presented for S_1 and Q_2 in Figures 10 and 11.

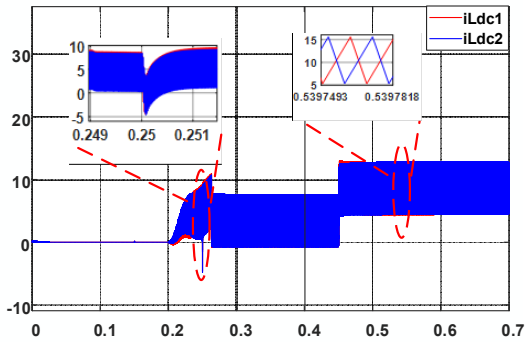

Fig. 8. Interleaved-boost current in simulation.

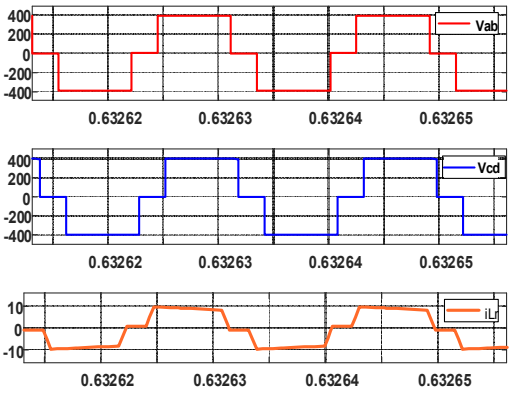

Fig. 9. Voltage on the two sides of the transformer and leakage current.

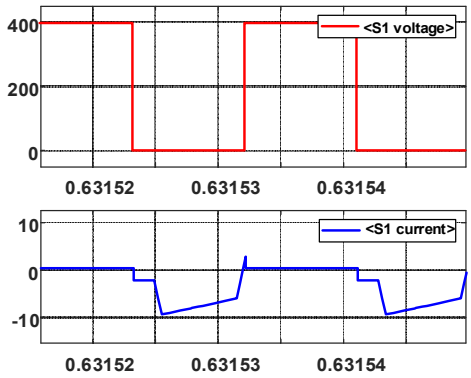

Fig. 10. Voltage and curent on switch device S_1.

III. CONCLUSION

The current paper presents the control structure along with the modeling of the CFDAB converter in boost mode. A small signal model is built up with the chosen modulation technique to control the output voltage of the converter. Simulations were carried out to verify both the proposed model and the control design. The simulation results prove the good performance of the control design not only in the steady-state but also in the dynamic responses.

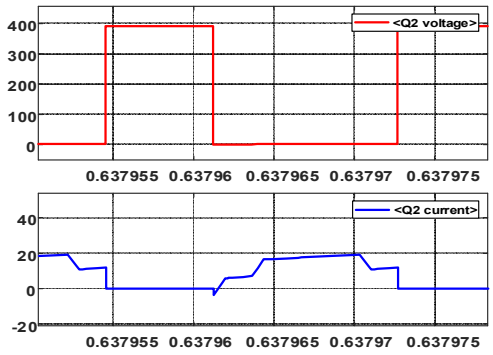

Fig. 11. Voltage and curent on switch device Q_2.

ACKNOWLEDGMENT

This research is funded by the Vietnamese Ministry of Education and Training under the project number CT2020.02.BKA.004.

REFERENCES

[1] W. Chen, X. Yang, W. Zhang, and X. Song, "Leakage Current Calculation for PV Inverter System Based on a Parasitic Capacitor Model," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8205–8217, Dec. 2016, https://doi.org/10.1109/TPEL.2016.2517740.

[2] Y. Almalaq and M. Matin, "Two-Switch High Gain Non-Isolated Cuk Converter," *Engineering, Technology & Applied Science Research*, vol. 10, no. 5, pp. 6362–6367, Oct. 2020, https://doi.org/10.48084/etasr.3826.

[3] K. Jayaswal and D. K. Palwalia, "Performance Analysis of Non-Isolated DC-DC Buck Converter Using Resonant Approach," *Engineering, Technology & Applied Science Research*, vol. 8, no. 5, pp. 3350–3354, Oct. 2018, https://doi.org/10.48084/etasr.2242.

[4] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014, https://doi.org/10.1109/TPEL.2013.2289913.

[5] B. J. Byen, B.-H. Jeong, and G.-H. Choe, "Single pulse-width-modulation strategy for dual-active bridge converters," *Journal of Power Electronics*, vol. 18, no. 1, pp. 137–146, Jan. 2018, https://doi.org/10.6113/JPE.2018.18.1.137.

[6] B. J. Byen, C.-H. Ban, Y.-B. Lim, and G.-H. Choe, "An efficiency-optimized modulation strategy for dual-active-bridge DC-DC converters using dual-pulse-width-modulation in the low power region," *Journal of Power Electronics*, vol. 17, no. 6, pp. 1413–1421, Nov. 2017, https://doi.org/10.6113/JPE.2017.17.6.1413.

[7] M. L. Mendola, M. di Benedetto, A. Lidozzi, L. Solero, and S. Bifaretti, "Four-Port Bidirectional Dual Active Bridge Converter for EVs Fast Charging," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, Sep. 2019, pp. 1341–1347, https://doi.org/10.1109/ECCE.2019.8912252.

[8] N. Hou and Y. W. Li, "A Tunable Power Sharing Control Scheme for the Output-Series DAB DC–DC System With Independent or Common Input Terminals," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9386–9391, Oct. 2019, https://doi.org/10.1109/TPEL.2019.2911059.

[9] D. Sha and G. Xu, *High-Frequency Isolated Bidirectional Dual Active Bridge DC–DC Converters with Wide Voltage Gain*, 1st ed. Berlin Heidelberg, Germany: Springer, 2018.

[10] A. K. Rathore and U. Prasanna, "Comparison of soft-switching voltage-fed and current-fed bi-directional isolated Dc/Dc converters for fuel cell vehicles," in *2012 IEEE International Symposium on Industrial Electronics*, Hangzhou, China, May 2012, pp. 252–257, https://doi.org/10.1109/ISIE.2012.6237093.

[11] A. Pressman, K. Billings, and T. Morey, *Switching Power Supply Design,* 3rd ed. New York, NY, USA: McGraw-Hill Education, 2009.

[12] Y. Shi, R. Li, Y. Xue, and H. Li, "Optimized Operation of Current-Fed Dual Active Bridge DC–DC Converter for PV Applications," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 6986–6995, Nov. 2015, https://doi.org/10.1109/TIE.2015.2432093.

[13] P. Xuewei and A. K. Rathore, "Small signal modeling of naturally clamped soft-switching current-fed dual active bridge dc/dc converter and control design using Cypress PSoC," in *2014 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Mumbai, India, Dec. 2014, https://doi.org/10.1109/PEDES.2014.7041961.

[14] A. Pal and S. Kapat, "Discrete-time Modeling of a Naturally Commutated Current-Fed Dual Active Bridge DC-DC Converter," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, Mar. 2019, pp. 2877–2881, https://doi.org/10.1109/APEC.2019.8722235.

[15] A. Pal and S. Kapat, "Accurate Discrete-Time Modeling of an Interleaved Current-Fed Dual Active Bridge DC-DC Converter," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, Mar. 2019, pp. 1616–1621, https://doi.org/10.1109/APEC.2019.8721870.

[16] D. Sha, X. Wang, K. Liu, and C. Chen, "A Current-Fed Dual-Active-Bridge DC–DC Converter Using Extended Duty Cycle Control and Magnetic-Integrated Inductors With Optimized Voltage Mismatching Control," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 462–473, Jan. 2019, https://doi.org/10.1109/TPEL.2018.2825991.