A Circuit for the Square Root of the Sum of Two Squared Voltages using an IC LM311 Open Collector Comparator

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***Abstract* — A circuit which accepts two input dc voltages V_1 and V_2 and provides an output dc voltage V_O equal to the square root of the sum of the two squared voltages of V_1 and V_2, using an LM311 open collector comparator based single quadrant time division multiplier is described in this paper.**

Keywords- generator; comparator; integrator; square rooter; adder

I. INTRODUCTION

A circuit for the square root of the sum of two squared voltages is often needed in instrumentation and control systems, particularly in phase sensitive detectors [1] which play an important role in impedance measurements and power measurements. This circuit is used in the construction of signal-envelope circuits, diversity combiner circuits, radiometer circuits and in other applications in which the powers of separate waveforms have to be added. Stern and Lerner described one circuit [2] in which they used a piecewise-linear network employing resistors and diodes. A different approach employing operational amplifiers, an LM 311 open collector comparator and switches is described here. The principle of the Time Division Multiplier [3-5] is used here in a simplified way.

II. CIRCUIT ANALYSIS

The proposed circuit diagram is shown in Figure 1. A sawtooth wave, marked as Vs in Figure 1, of peak value Vt is generated by the opamps OA1, OA2 and the switch S1. Let us assume that at start, the charge and hence voltage at the output terminal of opamp OA1 is zero. Since the inverting terminal of the opamp OA1 is at virtual ground, the current through R1, namely Vt/R1 Amps, would flow through and charge the capacitor C1. During the capacitor being charged (till the output of OA1 reaches a voltage level of Vt) the output of opamp OA2, configured to work as a comparator, will be at the LOW state and switch S1 is kept open (OFF). As soon as the output of OA1 crosses the level of Vt, say after a time period T, the output of comparator OA2 goes HIGH and the switch S1 is closed (ON). The switch S1 would then short the capacitor C1 and hence Vs drops to zero volts. After a very short delay time Td, required for the capacitor to discharge to zero volts, the comparator output returns to LOW and switch S1 is opened, thus allowing C1 to resume charging. This cycle, therefore, repeats itself at a period (T+Td). The waveforms at cardinal points in the circuit are shown in Figure 2.

The output of the integrator OA1 will be

$$Vs(t) = \frac{1}{R1C1}\int Vtdt = \frac{Vt}{R1C1}t \qquad (1)$$

From the waveforms shown in Figure 2 and the fact that at t=T, Vs(t) = Vt:

$$Vt = \frac{Vt}{R1C1}T$$

$$T = R1C1 \qquad (2)$$

The sawtooth wave Vs is compared with one input voltage V1 using the LM311 Comparator COMP1. The LM311 comparator has the characteristic that if the –ve input is greater than +ve input voltage, its output goes to LOW (pin no 1 has to be grounded). When the +ve input voltage is greater than the –ve input voltage, its output goes to the voltage at the other end of its pull up resistor Rp connected at the output [6]. Hence the output Vp1 of the comparator is a rectangular pulse waveform with a maximum value of the input applied voltage V1 as shown in Figure 2.

The ON time of the pulse waveforms vp1 is given by:

$$Ton1 = \frac{V1}{Vt}T \qquad (3)$$

The average value of Vp1 will be

$$Vw = \frac{1}{T}\int V1dt = \frac{V1}{T}Ton1 = \frac{V1^2}{Vt}$$

Similarly,

$$Vx = \frac{V2^2}{Vt}$$

.
$$Vy = \frac{Vo^2}{Vt}$$

$$-Vz = Vx + Vw$$

$$-Vz = \frac{V1^2 + V2^2}{Vt}$$

If R3=R4=R and R5>>R and considering KCL for node 'J' in the circuit of Figure 1, we get:

$$I1 = I2, \quad Vy = Vz, \quad \frac{Vo^2}{Vt} = \frac{V1^2 + V2^2}{Vt}, \quad Vo^2 = V1^2 + V2^2$$

$$Vo = \sqrt{V1^2 + V2^2} \qquad (4)$$

Thus the output voltage is the square root of sum of two (V1 and V2) squared voltages.

III. EXPERIMENTAL RESULTS

The circuit shown in Figure 1 was tested in our laboratory. LM 324 IC was used for OA1-OA8. CD 4053 IC is used for the switch S1. LM 311 ICs were used for COMP1-COMP3. Rp=1.2 kΩ, R1=1.2 MΩ and C1 = 10 nF. A voltage of ±7.5 V was chosen for the power supply. The test results are shown in Figures 3 and 4.

The accuracy of the circuit strongly depends upon the sharpness and linearity of the sawtooth waveform. The offset voltage of all the opamps used may cause a little error in the output and hence it must be adjusted to zero. The small variations in the voltage Vt will cause an error at the output, hence a stable precision reference voltage must be used as Vt. However, small variations in the power supply will not affect the performance of the circuit at all.

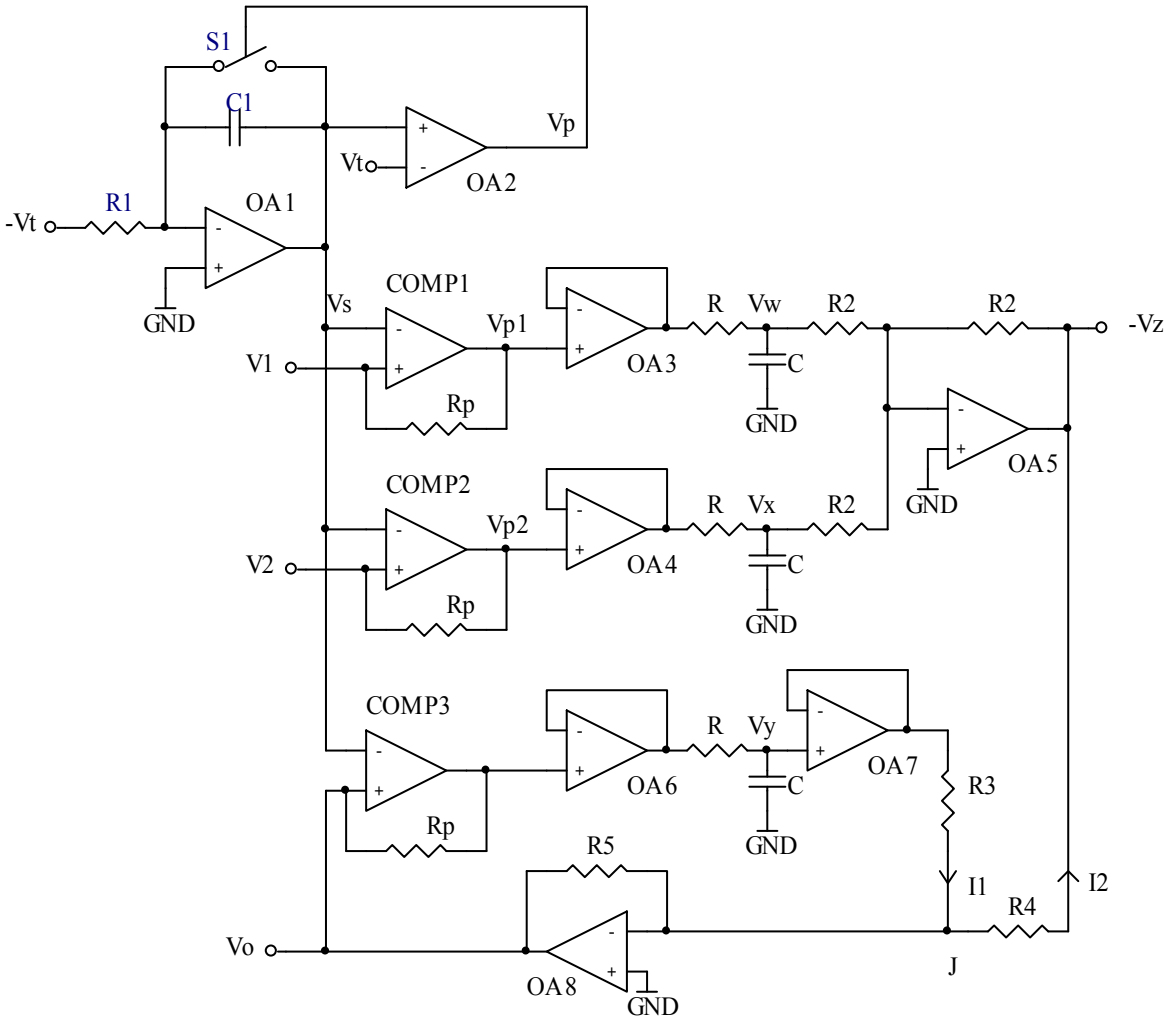

Fig. 1. Circuit diagram for the square root of the sum of two squared voltages

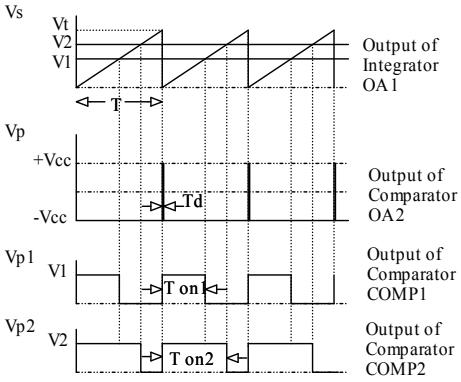

Fig. 2. Associated Waveforms of Figure 1

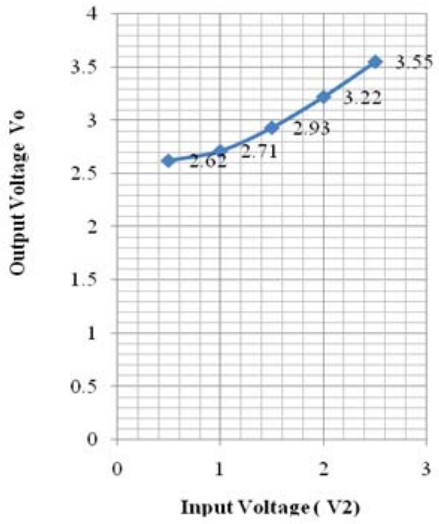

Fig. 3. Test results for Vt = 4V, V1 = 2.5V

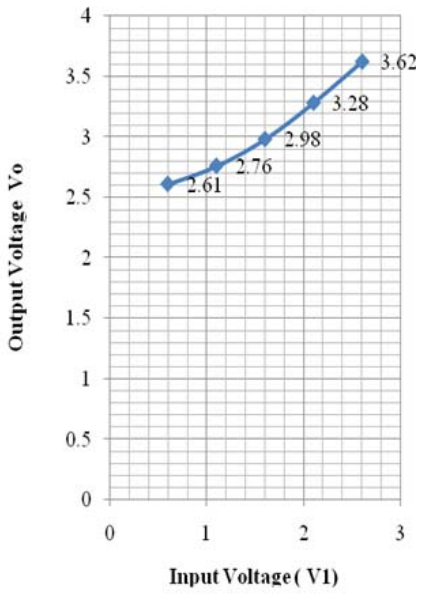

Fig. 4. Test results for Vt = 4V, V2 = 2.5V

ACKNOWLEDGEMENT

The author is highly indebted to Prof. S. Srinivasan, Prof. Dr. Enakshi Bhattacharya, Prof. Dr. V. Jagadeesh Kumar, Prof. Dr. Sridharan and Dr. Bharath Bhikkaji, Department of Electrical Engineering, Indian Institute of Technology, Madras, for their constant encouragement throughout the work. He also thanks Mrs. Latha Selvam for circuit drawing and discussions.

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K.C. Selvam was born on 2nd April 1968 in Krishnagiri District of Tamil Nadu State, India. He graduated from the Institution of Electronics and Telecommunication Engineers, (IETE) New Delhi, India in 1994. He has published more than 15 research papers in various national and international journals. He got the best paper award by IETE in 1996. At present he is working as Technical Staff in the Department of Electrical Engineering, Indian Institute of Technology, Madras, India. His research interests focus on measurements and instrumentation systems.