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ORIGINAL RESEARCH ARTICLE

# DESIGN OF Rf POWER AMPLIFIER FOR aDUAL-PURPOSE COMMUNICATION SATELLITE

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**ABSTRACT**

*This paper focuses on the design of RF power amplifiers for a dual-purpose communication satellite. The rapid growth in the use of power amplifiers for satellite communication is been documented. One of the major part of a high frequency communication system is the power amplifiers which amplifiers signals above 3GHz, into a frequency in the order of millions of cycles. The design of a radio frequency power amplifier is the most obvious solution to overcoming the battery lifetime limitation in the satellite communication system. This paper focuses on the design of a radio frequency amplifier with a technique to improve the drain efficiency of the class-F amplifier. This technique uses two passive networks; one of them is in series with the shunt capacitor Cs and the other in series with the MOSFET transistor's source terminal. The technique shows a significant improvement in the drain efficiency, which increases from 62% to 90%. This results to the demand for compact, low cost, and low power RF amplifiers. Thus, the design consideration was implemented, recorded, tested and met design specification*



## 1.0 Introduction

A dual purpose communication satellite can be used as Navigation Satellite and GPS. This creates a communication channel between a source transmitter and a receiver at different locations on earth. Dual purpose communications satellites find useful application for internet, television, telephone and military. The RF power amplifiers (PA) are used in a wide variety of applications including Wireless Communication, TV transmissions, Radar, and RF heating. The basic techniques for RF power amplification can use classes as A, B, C, D, E, and F, for frequencies ranging from VLF (Very Low Frequency) through Microwave Frequencies. RF Output Power can range from a few mW to MW, depending on application (More and Yadav 2016).

The introduction of solid-state RF power devices brought the use of lower voltages, higher currents, and relatively low load resistances (Li et al., 1984). The most important parameters that define an RF Power Amplifier are: Output Power, Gain, Linearity, Stability, DC supply voltage, Efficiency and Ruggedness. Choosing the bias points of an RF Power Amplifier can determine the level of performance ultimately possible with that PA. By comparing PA bias approaches, can evaluate the tradeoffs for Output, Power, Efficiency, Linearity, or other parameters for different applications. (Bin and Xingang 2014)

1.1 Literature Review

Traditionally, PAs are categorized into different classes according to their historical precedence. Different PA classes can be divided into two major groups: linear and non-linear PAs. Class A, AB, B and C PA are some of the well-known linear PAs, which are distinguished primarily by their bias condition. The Power Class of the amplification determines the type of bias applied to an RF power transistor. Linear PAs have the advantage of high linearity that is important for variable envelope modulation schemes (example4-QPSK) (Kazimierzet al., 2001). However, linear amplifiers suffer from poor maximum power efficiency which limits their applications in low power devices. In practice, an efficiency of only below 20% can be achieved in those systems. In contrast, non-linear PAs (also known as switched mode PAs) can achieve better efficiency. As suggested by its name, non-linear PAs have poor linearity performance. Nevertheless, it is still acceptable for constant envelope modulation schemes (example FSK). To overcome the problem of linearity to adapt to variable envelope systems, many linearization techniques have been proposed for non-linear amplifiers (Kazimierz et al., 2001). Therefore, due their high efficiency and the development of linearization techniques, non-linear PAs have received more attention over linear topologies in mobile communication in the last decade. Class E and F are the most common classes of non-linear PAs. In comparison, Table 1 shows the classes of PA and its comparison, Class E PA requires fast switching driver signal while Class F Pas does not require such. Moreover, because of relatively large switch stresses to active devices, (Tan et al., 2012) Class E amplifiers do not scale gracefully with the trend toward lower-power technology with lower breakdown voltage. For these reasons, (Yadav, 2016) Class-F PA has drawn more attention for its easier implementation and better integration with sub-micron CMOS technology.

Table 1: PA class comparison

| Class | Operation Mode | Angle of Conduction (%) | Drain Efficiency (%) |
|---|---|---|---|
| A | Current Source | 100% | 50% |
| B | Current Source | 50% | 78.5% |
| AB | Current Source | 50%-100% | 50%-78.5% |
| C | Current Source | <50% | 100% |
| D | Switch Mode | 50% | 100% |
| E | Switch Mode | 50% | 100% |
| F | Switch Mode | 50% | 100% |

The first CMOS RF power amplifier which delivered the hundreds of MW power reported in 1997, implemented on the single ended configuration with 0.8 μm CMOS Technology, the power amplifier was able to give 62% drain efficiency of (824~ 849) MHz using the supply voltage of 2.5V. The first GHz range differential power amplifier was reported in 1998, implemented using 0.35 μm CMOS Technology. In 2001, 130 nm CMOS technology came into notice, the main goals for the further improvement in the PA are as follows: (More and Yadav 2016).

High linearity to satisfy higher-order modulation scheme.

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Greater average output power level
Broader operating bandwidth
Low consumption of radio network energy reduces the environmental impact.

## 2.0 Methodology

Figure 1 shows the block diagram of the dual purpose amplifier. The figure was the foundation for the detailed design of the dual purpose amplifier.

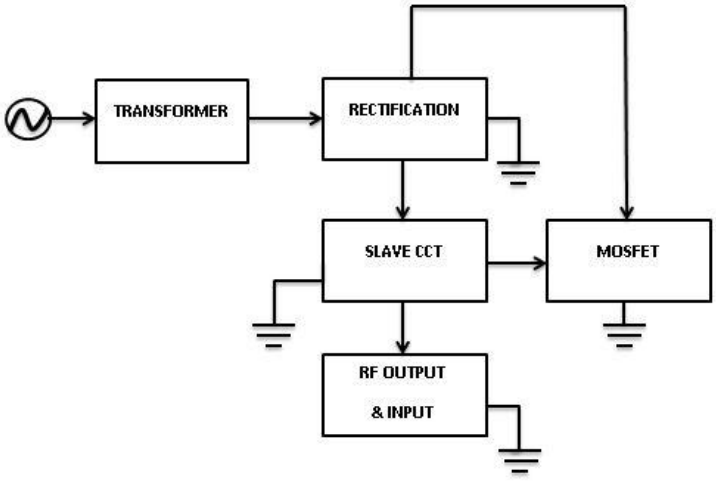


Figure 1: Block diagram of an RF power amplifier

Figure 2 is the Slave Circuit diagram for the dual-purpose amplifier. The circuit was design using resistor R20 value of 10/5w. This resistor and inductor L1 help in frequency modulation however; resistor R21 to R25 must use a uniform value of 10k in order to deliver maximum efficiency. The deliverable power of the PA lies on the numbers of N-channel and P-channel MOSFET. The implication of this is that increasing the numbers of MOSFET will automatically increase the efficiency. The values C10 and C12 was also consider as they are very significant in signal filtering process. The value of L1 (inductor was considerably chosen). In order to determine the failure rate of the dual purpose amplifier a reliability test was carried out using Parts Country Analysis.



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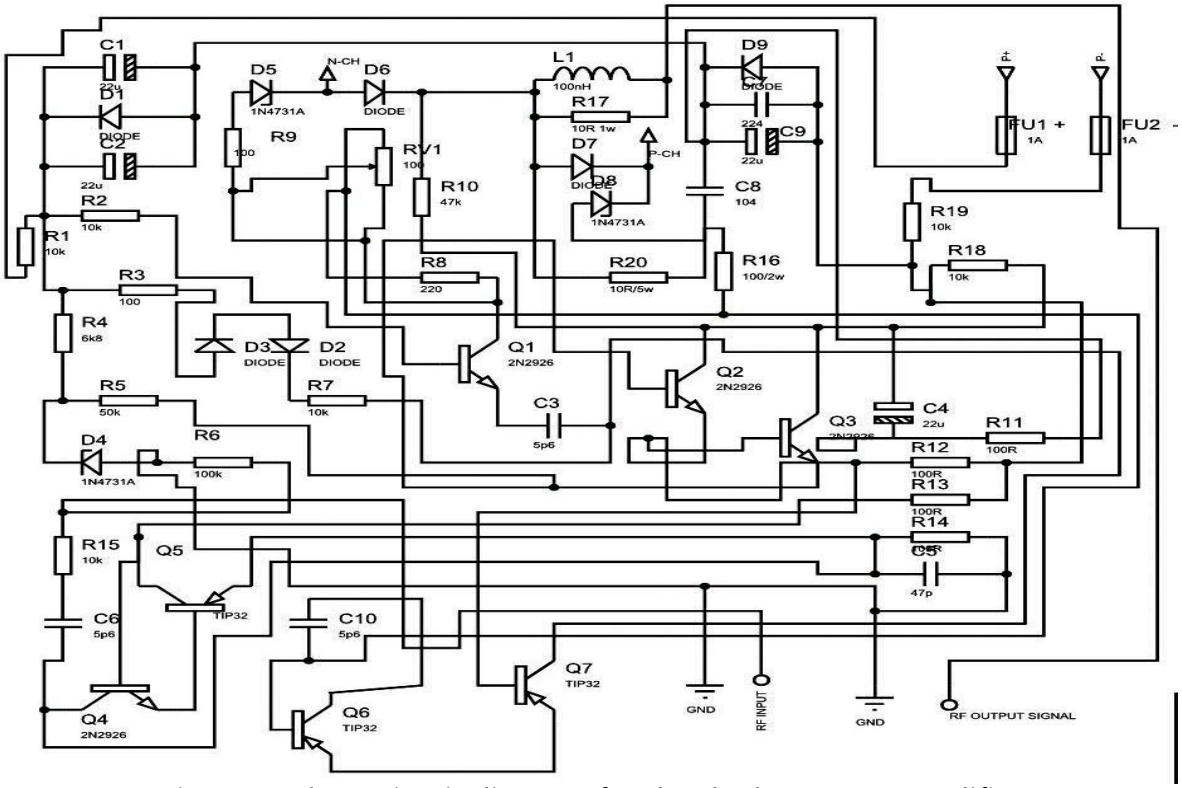


Figure 2: Slave Circuit diagram for the dual-purpose amplifier

## 2.1 Determination of input/output matching load line

The input matching configuration, including the bias circuit, has an important impact on the operation of the RF Power Amplifiers. This is because the input match will show different optima for maximum gain, best linearity, and highest efficiency. Optimization of the efficiency may involve substantial reduction in power gain. Correct handling of harmonics is a necessary feature on the input and the output match. Device used well below its cutoff frequency may require specific harmonic terminating circuit elements on the input.

The performance of the output matching circuit is critical for a Power Amplifier. In PA impedance control the amount of power delivered to the output is critical for maximum performance. This is in addition to the amount of gain and noise. This explains why matching network is critical for maximum performance. As aspect that is sometimes overlooked is the power dissipation design in the output matching circuit. This power is lost in the capacitors, inductors, and other loss elements that are part of the matching network. This "dissipation loss" degrades the PA's efficiency and output power capability. Different implementations of the output match results in different losses. It is worthy of note that there are still significant design tradeoffs to be made between bandwidth and dissipation loss. For a PA, the loss of the output match is always a concern because of the large power levels involved.

A capacitor's quality factor is inversely proportional to its capacitance (C). To minimize the dissipation loss of the output match, it is therefore necessary to design the output match with the lowest possible value of C. The tradeoff is between bandwidth and dissipation loss. Different capacitor technologies give different losses when used in

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output matching circuits.

One way of understanding the loss mechanisms of an output match is to simulate the match with loss-less components, then introduce loss into one component at a time.

$$\text{Mismatch Loss[dB]} = 10*\text{LOG}\,(1-\Gamma 2) \quad (1)$$

$$\text{Where reflection coefficient } \Gamma = \frac{(\text{VSWR}-1)}{(\text{VSWR}+1)} \quad (2)$$

VSWR is the Voltage Standing Wave Ratio, which is the measure of how efficiently radio-frequency power is transmitted from a power source, through a transmission line, into a load.

Because the dissipation loss does not depend on the source impedance it is possible to use S21 to find the correct dissipation loss in a circuit simulation. The procedure involves using the complex conjugate of the simulated load line as the source impedance. Running at a low efficiency not only reduces talk time in a portable device, but it also creates significant problems with heating and reliability. The load line is set based on the needed Power Amplifier output power and available supply voltage.

$$RL = \frac{\text{Vmax}}{\text{Imax}} \quad (3)$$

Where RL is the impedance load.

Matching for maximum Gain occurs when the amplifier is unconditional stable and load impedance is equal to the complex conjugate of the same source impedance (conjugate matching). Complex conjugate simply refers to complex impedance having the same real part with an opposite reactance. Figure 3 shows the input and output matching diagram. e.g. - if the source impedance is Zs=R+jX, then its complex conjugate would be Zs*=R-jX

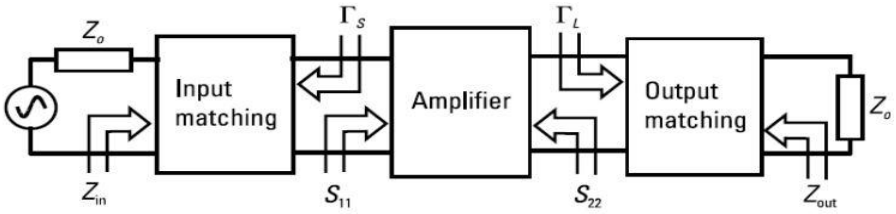


Figure 3: Input and output matching

If matched: $Z_{in} = Z_o$, $\Gamma_s = S_{11}^*$, and $Z_{out} = Z_o$, $\Gamma_L = S_{22}^*$

Matching for maximum Output Power occurs when Optimum Load impedance (RL) is equal to Source impedance (Rgen). In order to obtain maximum output power, typically the power amplifier is not conjugate matched. Instead, the load is designed such that the amplifier has the correct voltage and current to deliver the required power. If operation is at the optimal Power Added Efficiency point, optimal-power tuning produces about 1 dB to 3 dB of higher power. Gain is reduced (for small Pin) typically by a slightly smaller amount. The transistor ' s input and output impedances will also decrease with an increase in frequency, which further complicates the design of a PA's matching networks, especially since these impedances can be as low as 0.5 Ω. Thus,



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when matching a discrete driver stage to its PA with maximum efficiency, we would normally want to implement a direct match from the true output impedance of the driver to the true input impedance of the PA, instead of first forming a 50-Ω match at the output of the driver, and then another 50-Ω match for the input of the power amplifier, as this would needlessly transform the impedances from low to high, and then back from high to low. By selecting a transistor with a high collector voltage requirement, output impedance can be increased over a transistor that operates at lower values of collector voltage.

## 3.0 Results and Discussion

From Figure 2, the input signal of the slave circuit for the power amplifier is processed and filter through the slave circuit and then passed to the amplification stage, the amplification is done with the aid of P-channel and N-channel MOSFET. In the circuit diagram P+ and P- is the input power supply from the rectified DC source and the ground terminal. However, two fuses FU1 and FU2 were connected to the input terminal of the slave circuit to protect the circuit from over voltage surge. The design was analyzed and simulated using LTspice electronic software as shown below.

Figure 4 shows that there is a rise in voltage (gain) with time, this means that at every instant of time the power amplifier experiences an increase in voltage, and however an increase in voltage is an increase in gain. This is in agreement with the result of a study on Comparative Study of Audio Amplifiers (Vimal Raj et al., 2017).

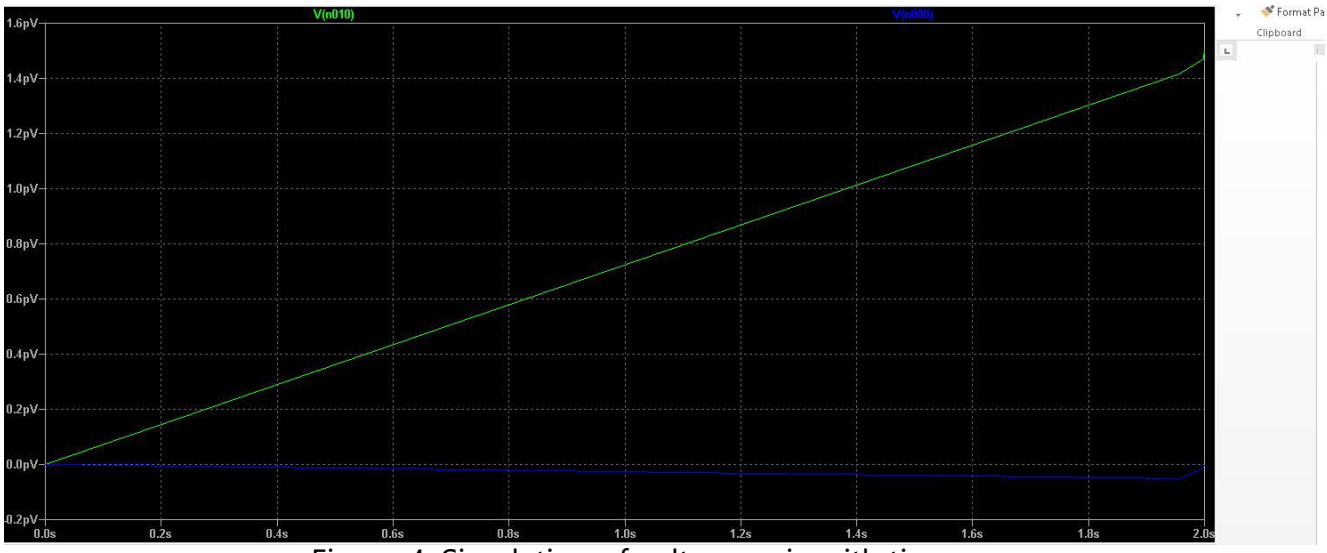


Figure 4: Simulation of voltage gain with time

### 3.1 Reliability Calculation of this Model using Parts Country Analysis

Table 2 shows the component used in calculating the failure rate of the system, the total failure rate of the device is 1.057854 x 10-6per hour.

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Table 2: Estimation of failure rate in the circuit

| Component/Part | No of Similar Parts | $\lambda_g$ (x$10^{-6}$) | Total Failure rate (x$10^{-6}$) Per hour |
|---|---|---|---|
| Power Transistors FET | 8 | 0.014 | 0.112 |
| Low power transistor | 2 | 0.0560 | 0.112 |
| NPN & PNP transistors | 4 | 0.00015 | 0.0006 |
| Zener diode | 2 | 0.0110 | 0.022 |
| Resistor, o.1 Watt | 19 | 0.0115 | 0.2185 |
| Resistor, Film | 5 | 0.0323 | 0.1615 |
| Capacitor, electrolytic | 6 | 0.0540 | 0.324 |
| Ceramic capacitor | 5 | 0.0035 | 0.0175 |
| Inductor, fixed | 2 | 0.000032 | 0.000064 |
| (General purpose) Diode | 9 | 0.0036 | 0.0324 |
| switching | 1 | 0.00094 | 0.00094 |
| RF Coaxial | 1 | 0.00045 | 0.00045 |
| Hand solder | 43 | 0.0013 | 0.0559 |
| | | | Σ = 1.057854 |

$$\lambda_{eqpt} = \sum_{i=1}^{n} N_i \lambda_{gi} \pi_{Qi} \quad (4)$$

Where:

$\lambda_{eqpt}$ = total equipment failure rate (failure per $10^6$ hours),

$\lambda_{gi}$ = generic failure rate for the i-the generic part (failures per $10^6$ hours,

$\pi Qi$ = quality factor for the i-the generic part,

$N_i$ = quality of i-the generic part,

N = number of different generic part categories in the equipment.

Figure 5 shows the Power MOSFET (Amplification drivers Circuit diagram) this circuit uses E-MOSFET shown in figure 6, which must have VGS greater than the threshold value (VGS (th)) so that zero bias cannot be used. From equation (5) VG can be determined. This method of E-MOSFET bias is equivalent to collector – feedback bias in transistor Figure 6(i) shows the drain-feedback bias circuit for n-channel F-MOSFET. This is in agreement with an earlier work on CMOS based current feedback OP-AMP with improved bandwidth (Akshay2015). A high resistance RG is connected between the drain and the gate. Since the gate resistance is super high, no current will flow in the gate circuit (i.e. IG = 0). Therefore, there will be no voltage drop across RG. Since there is no voltage drop across RG, the gate will be at the same potential as the drain. This fact is illustrated in the DC equivalent circuit of drain-feedback bias as in Figure 6(ii)

$$V_D = V_G \quad \text{and} \quad V_{DG} = V_{GS} \quad (5)$$

Where;

$V_D$ = Drain Voltage

$V_G$ = Gate Voltage

$V_{DG}$ = Voltage along Drain and Gate terminal

$V_{GS}$ = Voltage along Gate and Source



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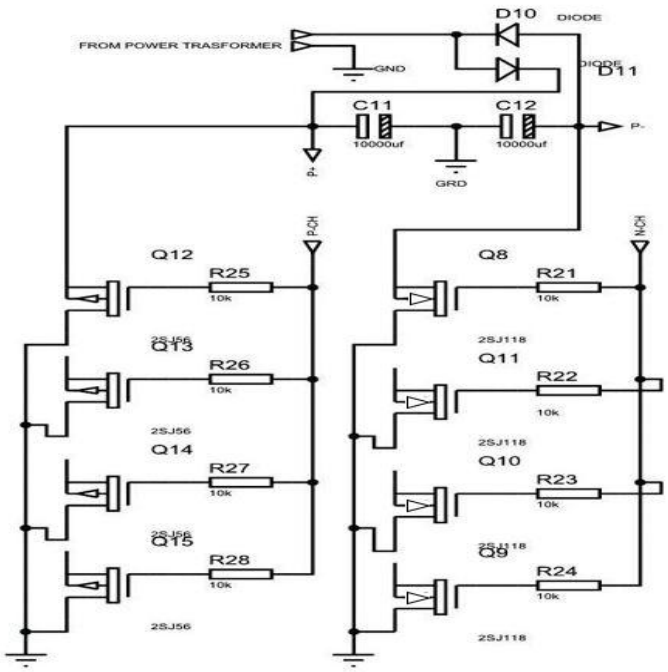


Figure 5: Power MOSFET (Amplification drivers)

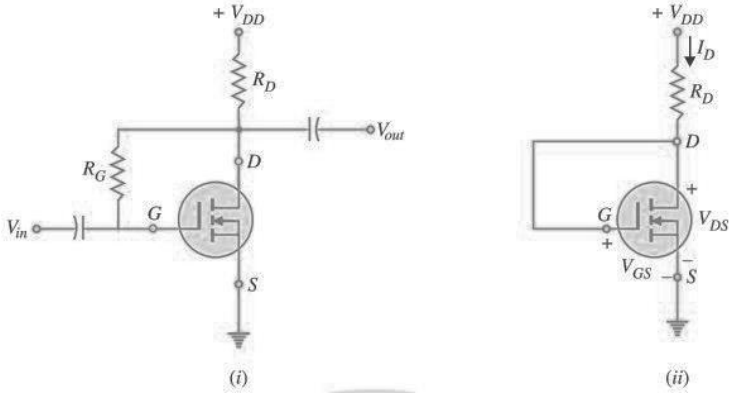


Figure 6: Feedback bias transistor

The value of drain-source voltage $V_{DS}$ for the drain-feedback circuit is

$$V_{DS} = V_{DD} - I_D R_D \quad (6)$$

Since $V_{DS} = V_{GS}$ , $V_{GS} = V_{DD} - I_D R_D$
Since in this circuit $V_{DS} = V_{GS}$ , $I_D = I_{D(on)}$
Therefore, the Q-point of the circuit stands determined.

From the calculation, the RF Power Amplifier for the Proposed Dual Purpose Communication Satellite was successfully designed and developed as shown in Figure 8. .The circuit diagram was then printed on a PCB as shown in the layout in figure 9. A prototype of the dual purpose amplifier was then assembled and integrated as shown in figure 10. The prototype was tested at the Centre for Satellite Technology Development, Abuja. The tests include reliability test and calculation for this design. The results are in agreement with the finding of a study on the Comparative Study of Audio Amplifiers (Vimal Raj et al., 2017).

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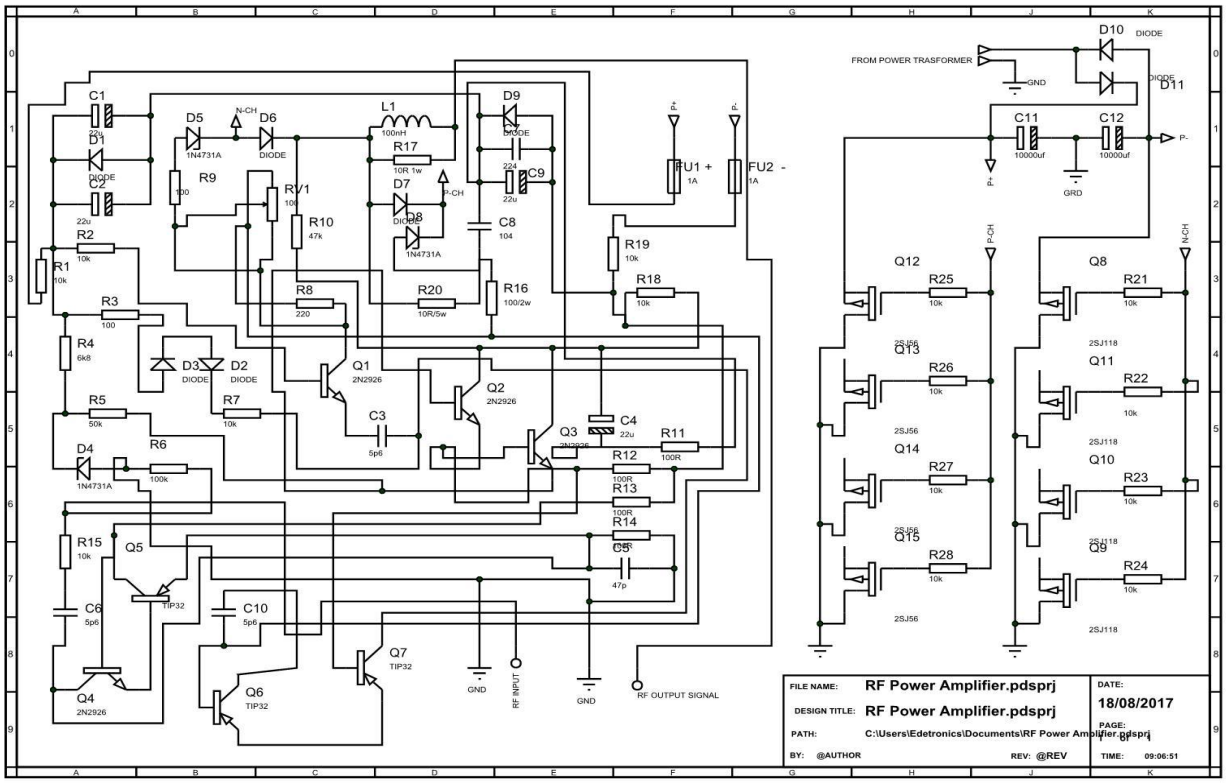


Figure 8: Complete circuit diagram of an RF Power Amplifier

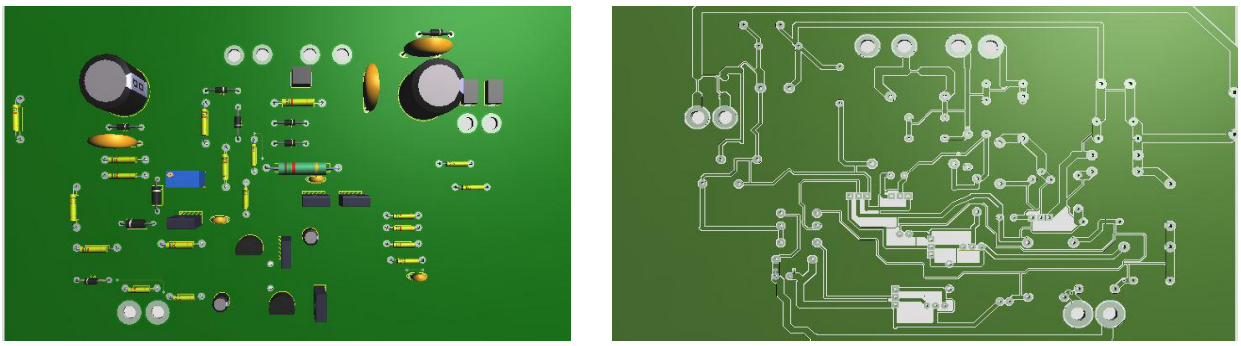

Figure 9: PCB design layout

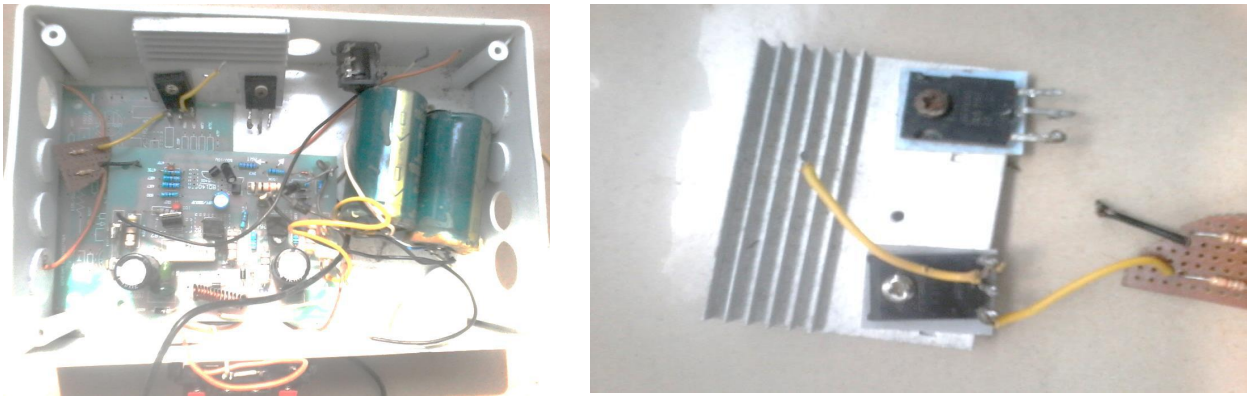

Figure 10: Finished prototype RF power amplifiers for the proposed dual purpose communication satellite



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## 4.0 Conclusion

In this paper, some recent developments of Class-F power amplifiers are presented, especially on their integration with deep sub-micron CMOS technology. This result is a significant step in the design of a dual purpose amplifier for Communication Satellite in order to achieve low cost and efficient power amplifier. In addition, many issues are still needed to be resolved before the goal of System-on-a-Chip can be realized. Nevertheless, the rapid growing demand of mobile communication devices will be a good catalyst for the development of RF power amplifiers and a real SOC solution will hit the market very soon in the future.

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