Implementation of a Power Combining Network for a 2.45 GHz Transmitter Combining LINC and EER

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A power combining network with 180N hybrid for a 2.45 GHz Transmitter Combining LINC and EER has been analyzed, built and measured. The network feeds the wasted outphasing power partly back to the power supply and therefore improves the overall power efficiency. The recycling circuit was designed and simulated with ADS. A measured peak recycling efficiency of 60% was achieved with commercial Schottky diodes at 2.45 GHz at an input power of 36 dBm.

1 Introduction

Power efficiency and linearity are two important properties in conventional linear amplifier design and cannot be achieved simultaneously. Linear amplification with nonlinear components (LINC [1]) can produce output signals with high linearity after combining the antiphase outputs of two nonlinear power amplifiers. Envelope elimination and restoration (EER [2]) is an approach for high efficiency amplification. Due to the class-S power amplifier which acts as a power supply for the output power amplifier of EER, EER is limited to a signal with bandwidths up to serveral MHz. The combination of LINC and EER (CLIER [3]) takes advantage of three nonlinear power amplifiers to achieve linear amplification. The inherent characteristic of this architecture allows power amplifiers to continuously operate at their peak power efficiency, and potentially improves the overall efficiency of the system. The structure is shown in Fig. 1. However, a major disadvantage of this approach is the power wasted when the two power amplifiers are outphasing if a conventional 180° hybrid is used as a combiner. An alternative combining approach, named after Chireix and extensively analyzed in [4], suffers from incomplete isolation of the two Class-E power amplifiers. The two amplified signal components tend to travel and reflect back and forth between two amplifier branches, and the two amplifiers appear to be interfering with each other. As a result, a significant signal distortion can occur. In this paper,

a different approach is presented and designed – the hybrid approach with a rat race coupler is used, but the power recycling scheme simply takes a RF-DC converter to recycle part of the wasted power back to the battery and enhance power efficiency. The focus of this paper is on the recycling network.

2 Theory

The baseband source signal of CLIER $S(t)$ can be written as

$$S(t) = a(t)\, e^{j\varphi(t)},\, a(t) \geq 0, \tag{1}$$

where $a(t)$ is the envelope of the baseband input signal and $e^{j\varphi(t)}$ describes the phase of the baseband input signal. The envelope of the input signal is digitally low pass filtered. The resulting signal $a_1(t)$ is amplified using a highly efficient class S amplifier.

The quotient of the envelope $a(t)$ and the lowpass filtered envelope $a_1(t)$ and the original phase of the signal are now amplified via the LINC principle. The resulting out-phasing phase $\psi(t)$ is given by

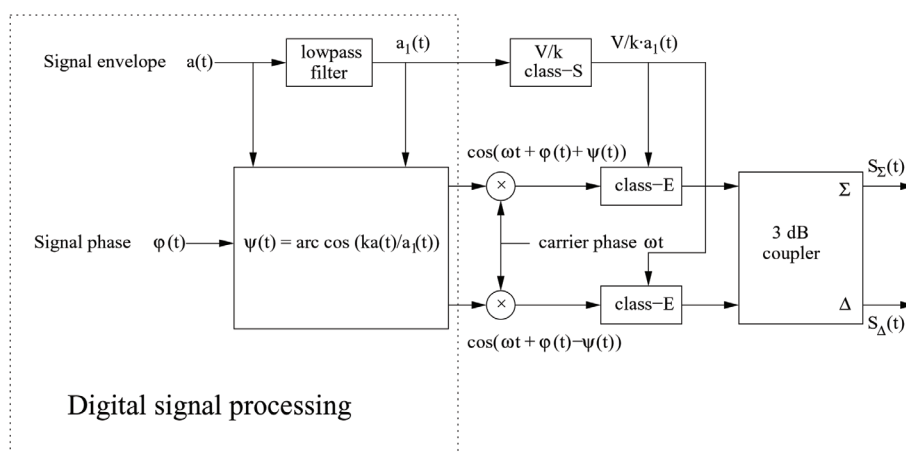$$\psi(t) = \arccos\left(\frac{k\, a(t)}{a_1(t)}\right). \tag{2}$$

Fig. 1: Block diagram of CLIER principle

Note that the argument of the arccosine is limited to ± 1, and if the limits are exceeded, clipping occurs. The amount of clipping is determined by the clipping factor k, the lower part of the envelope $a_1(t)$ is fed to the class E amplifier via the supply voltage restoring the lower part of the envelope.

The baseband representation of the signal is then after the DSP the resulting LINC signals can be written as

$$S_1(t) = \frac{Va_1(t)}{2k} \exp(\varphi(t) + \Psi(t)), \tag{3}$$

$$S_2(t) = \frac{Va_1(t)}{2k} \exp(\varphi(t) - \Psi(t)). \tag{4}$$

These two signals are fed into a 3 dB combiner. If the two amplifier branches are perfectly matched, i.e., their gain and phase characteristics are precisely the same, an amplified replica of the original signal can be achieved, as the in-phase components add together and the out-of-phase components cancel each other. In this case the desired output signal is obtained at the summing port. The differential portion of the power is consumed at the resistive load and turns into waste heat, which degrades the overall power efficiency of CLIER. An important figure of merit of a LINC based system is the average output efficiency, which can be expressed as

$$\eta_O = \frac{\overline{S_\Sigma(t)}^2}{\overline{S_\Sigma(t)}^2 + \overline{S_\Delta(t)}^2}, \tag{5}$$

where $S_\Sigma(t)$ and $S_\Delta(t)$ are the in-phase components and out--phase components of $S_1(t)$ and $S_2(t)$, respectively. It describes how much of the produced power is used at the output. In this paper a technique for partial recovery of the wasted power at the differential port is implemented. The isolation between the two amplifiers is not degraded. This new technique was called power recycling or re-use technique in [5, 6]. The idea
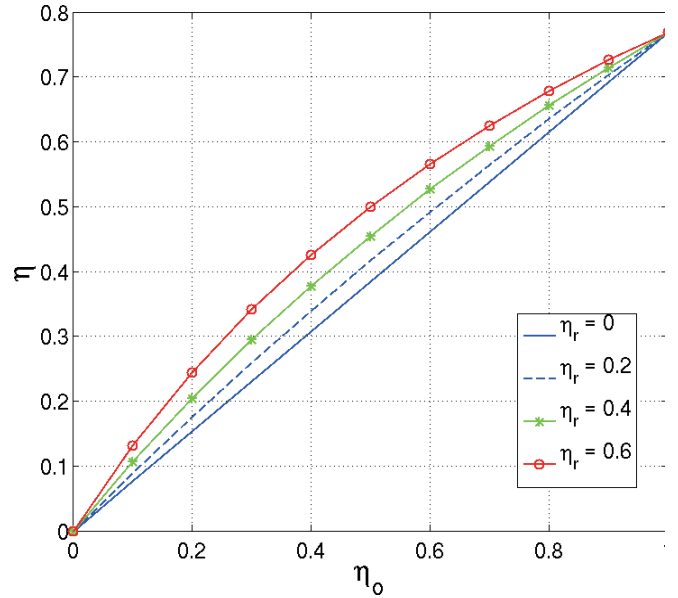

Fig. 2: Efficiency depending of tha output efficiency η_O and the recycling efficiency η_R. The other values are $\eta_C = 0.95$, $\eta_E = 0.9$, $\eta_S = 0.9$.

is simple – replace the power wasted resistive load with a RF-DC converter to recover the wasted power back to the power supply, and hence improve the overall power efficiency of the amplifier system. Then the overall efficiency of the entire CLIER system can be written as

$$\eta = \frac{P_\Sigma}{P_{DC}} = \frac{\eta_O \eta_C \eta_E \eta_S}{1 - (1 - \eta_O)\eta_C \eta_E \eta_S \eta_R} \tag{6}$$

in which η_O, η_C, η_E, η_S, η_R are the output efficiency, the efficiency of the combiner, the efficiency of the class E amplifier, the efficiency of the class S amplifier and the efficiency of the recycling network respectively. The total efficiency in dependency on the output and the recycling efficiency is shown in Fig. 2. We can see that the system efficiency depends on the
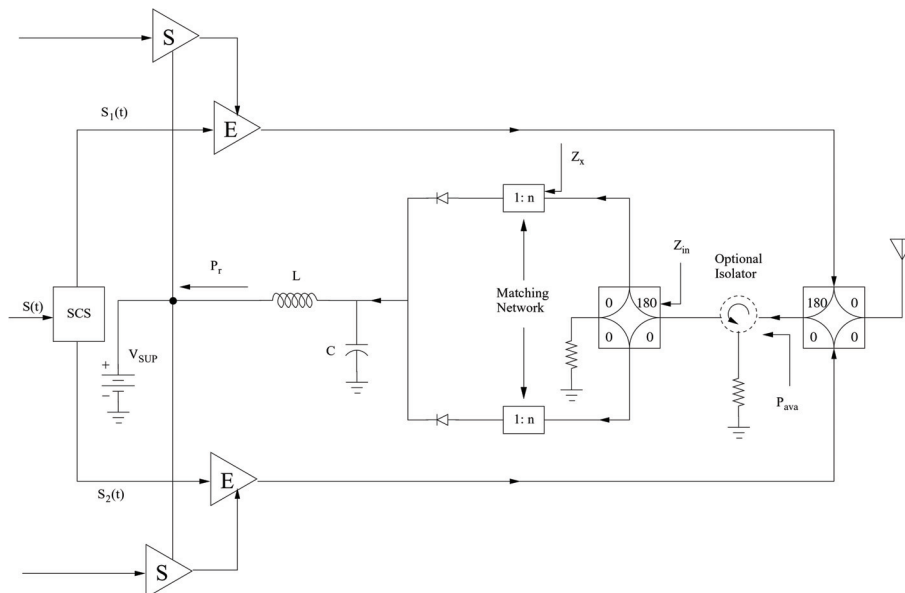

Fig. 3: Outphasing power amplifier with power recycling

output efficiency. The system efficiency increases significantly with recycling for medium η_O. A diagram of this recycling approach is illustrated in Fig. 3. A 180° hybrid combiner is configured as the power splitter to divide the wasted power into two 180° outphased portions. These two signals are then fed to a high-speed Schottky diode pair through an impedance matching network. The Schottky diodes rectify the RF waves and the DC components are withdrawn back to the power supply. A large value shunt capacitor and/or a series inductor may be used to reject the harmonic currents. The matching network is to be adjusted to optimize the system performance. An optional isolator can be added between the hybrid combiner and the power splitter to improve the isolation. Apparently, the simplest case is that the input signal is a continuous wave, where the signal magnitude is constant. To simplify the analysis, an ideal resistive model is assumed for the Schottky diode, i.e. the fixed on-resistance Rd in series with the built-in potential Vd, the infinite off-resistance, and a negligible shunt capacitance. All other components are assumed ideal. The analysis starts from the diode side. Each Schottky diode conducts at an angle of 2θ. The current though the upper diode can be written in the following form[6]:

$$I_{d1}(t) = \begin{cases} \dfrac{V_{pk}\cos\omega_c t - (V_{\mathrm{sup}} + V_d)}{R_d}; & \cos\omega_c t \ge \dfrac{(V_{\mathrm{sup}} + V_d)}{V_{pk}} \\ 0; & \text{otherwise,} \end{cases} \quad (7)$$

where V_{pk} is the peak signal voltage applied to the diode, V_{sup} is the power supply voltage and ω_c is the carrier frequency of the input signal. So the upper diode conduction angle θ can be determined by

$$\cos\theta = \frac{V_{\mathrm{sup}} + V_d}{V_{pk}}; \quad 0 \le \theta \le \frac{\pi}{2}. \quad (8)$$

The input signal is a periodic function with a period of 2π. In the actual circuit, the transmit signal is not only a signal with one carrier frequency (fundamental frequency), but also a sum signal of higher order frequencies (harmonic frequencies) because of the non linearity of the recycling network. So the actual diode current can be written as a Fourier series. For the simplest case, the diode current can be expanded as the following Fourier series

$$I(t) = i_0 + \sum_{k=1}^{\infty} i_k \cos(\omega_c t), \quad (9)$$

where i_k is the kth-order harmonic of the diode current. The DC-component of the upper diode is thus given by

$$I(0) = \frac{V_{\mathrm{sup}} + V_d}{\pi R_d}(\tan\theta - \theta). \quad (10)$$

The fundamental component and the higher order harmonics of the upper diode current are

$$I(k) = \frac{V_{\mathrm{sup}} + V_d}{\pi R_d \, k\cos\theta}\left[\frac{\sin(k-1)\,\theta}{k-1} - \frac{\sin(k+1)\,\theta}{k+1}\right]. \quad (11)$$

Obviously, the fundamental components and all odd-order harmonic current of the two diodes are 180° out of phase, and hence cancel out. Only the DC components and even-order harmonics are left. A large value shunt capacitor may be sufficient to short the harmonic currents to the ground. A series inductor may be added to better help reject the harmonic current out of the power supply. In practice, microstrip lines are used instead of the capacitor. The recycled portion of the power is hence

$$P_r = 2\,i_0 V_{\mathrm{sup}}. \quad (12)$$

The RF-DC conversion is a strongly nonlinear process. In such a case, the large signal impedance of the device is usually estimated by the fundamental component of the voltage and current waveforms. The fundamental component of the upper diode current at carrier frequency is

$$i(1) = \frac{V_{\mathrm{sup}} + V_d}{\pi R_d}(\theta\sec\theta - \sin\theta). \quad (13)$$

The available power to the recycling network needs to be known in order to calculate the recycling efficiency. An isolator can be placed between the two hybrids to eliminate the reflection wave back to the two power amplifiers. Now looking from the first hybrid (see Fig. 3), the load is always matched to 50 Ω, while looking from the seconde hybrid, the isolator acts like an ideal voltage source V_s in series with an internal resistance of 50 Ω. Thus the source voltage is

$$V_s = V_1 + Z_0 I_1 = \sqrt{2}\,n V_{pk} + \sqrt{2}\,\frac{Z_0 i_1}{n}, \quad (14)$$

where the scaling factor n results from the $1:n$ matching network and $\sqrt{2}$ comes form the fact that the hybrid is a power addition device. The power available to the recycling network P_{ava} is

$$\begin{aligned} P_{ava} &= \frac{1}{8}\frac{V_s^2}{Z_0} \\ &= \frac{(V_{\mathrm{sup}} + V_d)^2}{4Z_0}\cdot\left[n\sec\theta + \frac{Z_0}{n\pi R_d(\theta\sec\theta - \sin\theta)}\right]^2. \end{aligned} \quad (15)$$

So the recycling efficiency is

$$\eta_r = \frac{P_r}{P_{ava}}. \quad (16)$$

If we only account for the fundamental components, we can obtain the input impedance of the recycling network

$$Z_{in} = n^2\frac{V_{pk}}{i(1)} = \frac{n^2\pi R_d}{\theta - \sin\theta\cos\theta}. \quad (17)$$

So the input impedance of the recycling network and the recycling efficiency vary with the diode conduction angle,
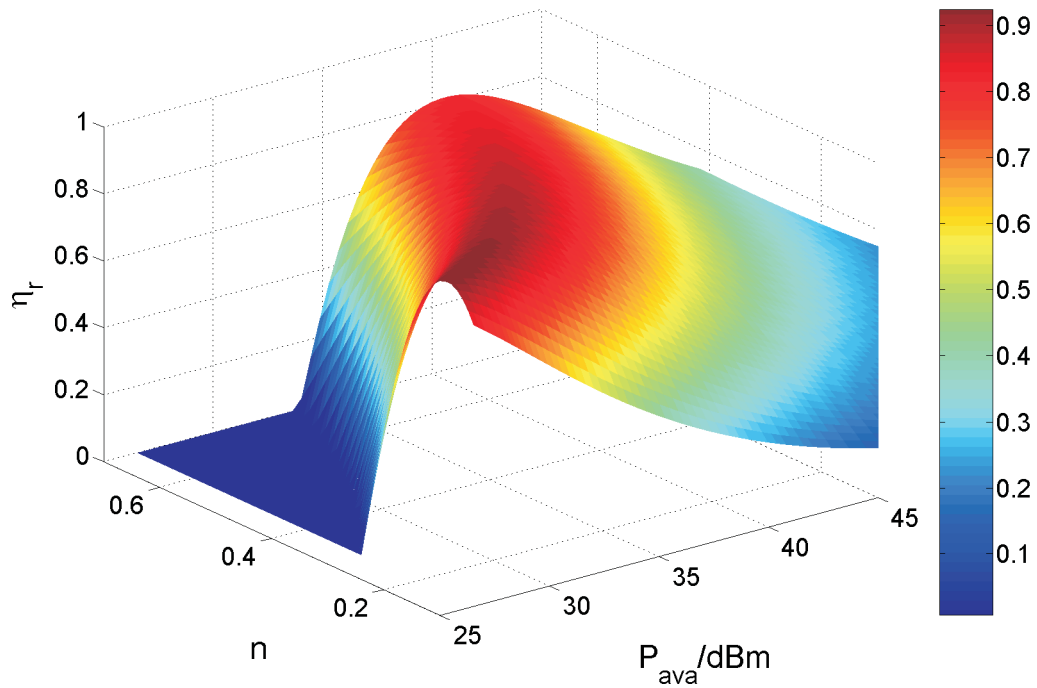
Fig. 4: Recycling efficiency as a function of n and available power

which is in fact determined by the power delivered to the recycling network. The reflection coefficient of the recycling network is

$$\Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}. \tag{18}$$

The $V\,SWR$ is thus, according its standard definition

$$V\,SW\,R = \frac{1 + |\Gamma_{in}|}{1 - |\Gamma_{in}|}. \tag{19}$$

Fig. 4 and Fig. 5 show the 3D plots of the recycling efficiency and reflection coefficient as a function of the impedance transform ratio n of the matching network and the source available power Pava with the following parameters: $V_{sup} = 30$ V, $V_d = 1.6$ V and $R_d = 4.8$ Ω. It is clear that there is a close relationship between the optimum recycling efficiency and the lowest reflection coefficient.
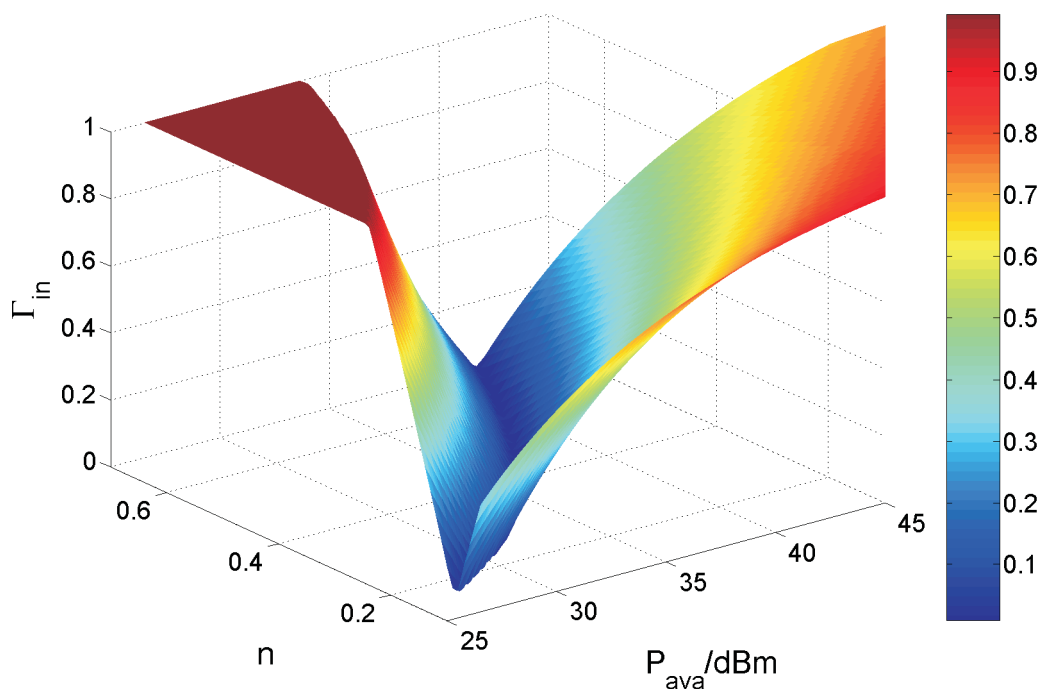

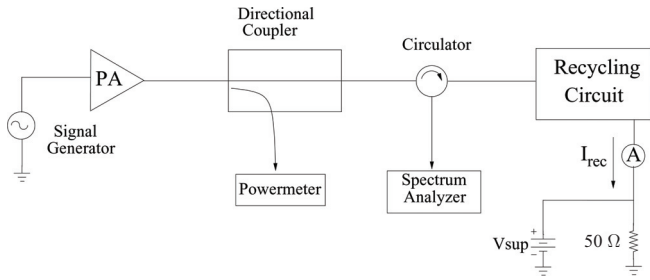Fig. 5: Reflection coefficient as a function of n and available power

Fig. 6: Diode detector test setup

Fig. 7: Photograph of the measured circuit optimized for 36 dBm

3 Measured results and discussion

The power recycling circuit and the 180° hybrid ring coupler of Fig. 3 were designed and simulated with Advanced Design System (ADS) and fabricated on RT/Duroid 5880. The measurement setup is illustrated in Fig. 6. The power amplifier is used to provide the proper power level to the recycling network, since the signal generator is not capable of delivering so much power. The directional coupler is used to monitor the input power into the recycling network via the power meter. The circulator is used to isolate the power amplifier and the recycling network and enables the measurement of the reflected power using the spectrum analyzer. The external load simulates the power dissipation of the Class-S power amplifier. The center frequency used for all tests is 2.45 GHz. The DC current I_{rec} is measured and the recycled power calculated. For all measurements the supply voltage is kept fixed at 30 V (25 V, 20 V) and the input power level is varied to determine the power recycling efficiency. One of the recycling circuits is optimized at 36 dBm input power for 30 V power supply voltages with surface mount Schottky diodes
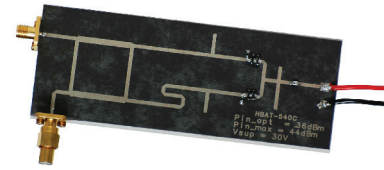
(HBAT540C). The layout of this circuit is shown in Fig. 7. Fig. 8 and 9 show the measured results for recycling efficiency and measured reflection coefficients as a function of the input power for three different power supply voltages. The measured peak recycling efficiency is found to be 57.13 % for a supply voltage of 20 V, 61.88 % for a supply voltage of 25 V and 60.9 % for a supply voltage of 30 V. In order to test the band width, the supply voltage and the input power level were kept constant and the frequency was swept. The result is shown in Fig. 10. The band width for this circuit is about 100 MHz. Another is optimized at 41 dBm input power for 30V power supply with the surface mount Schottky diodes group (HSMS280E). The measured peak recycling efficiency is found to be 62.7 % for 20 V supply, 63.4 % for 25 V supply, and 63.7 % for 30 V supply.

4 Conclusion

The power recycling technique has been presented for the optimum power combining network of the CLIER system. This network acts as an RF-DC converter while maintaining sufficient isolation. The analysis demonstrates that a proper trade-off among the diodes, the power supply and the input power of the recycling networks is critical for the performance
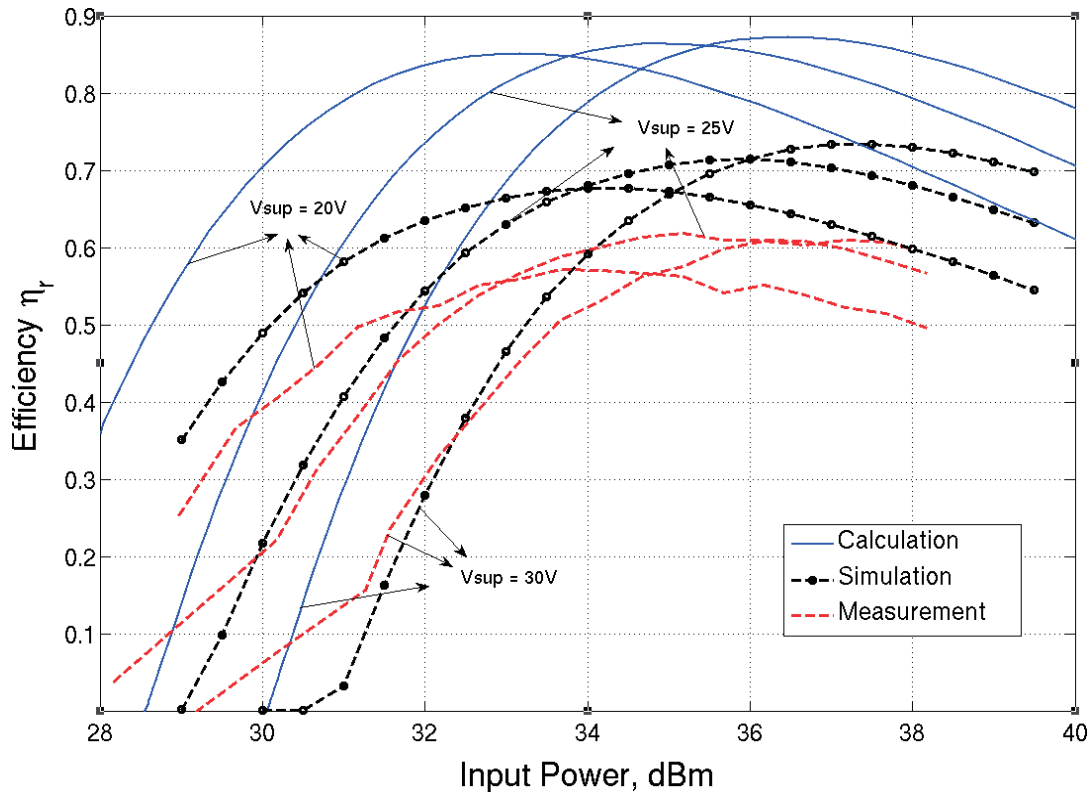

Fig. 8: Comparison of calculated, simulated and measured recycling efficiency as a function of input power level
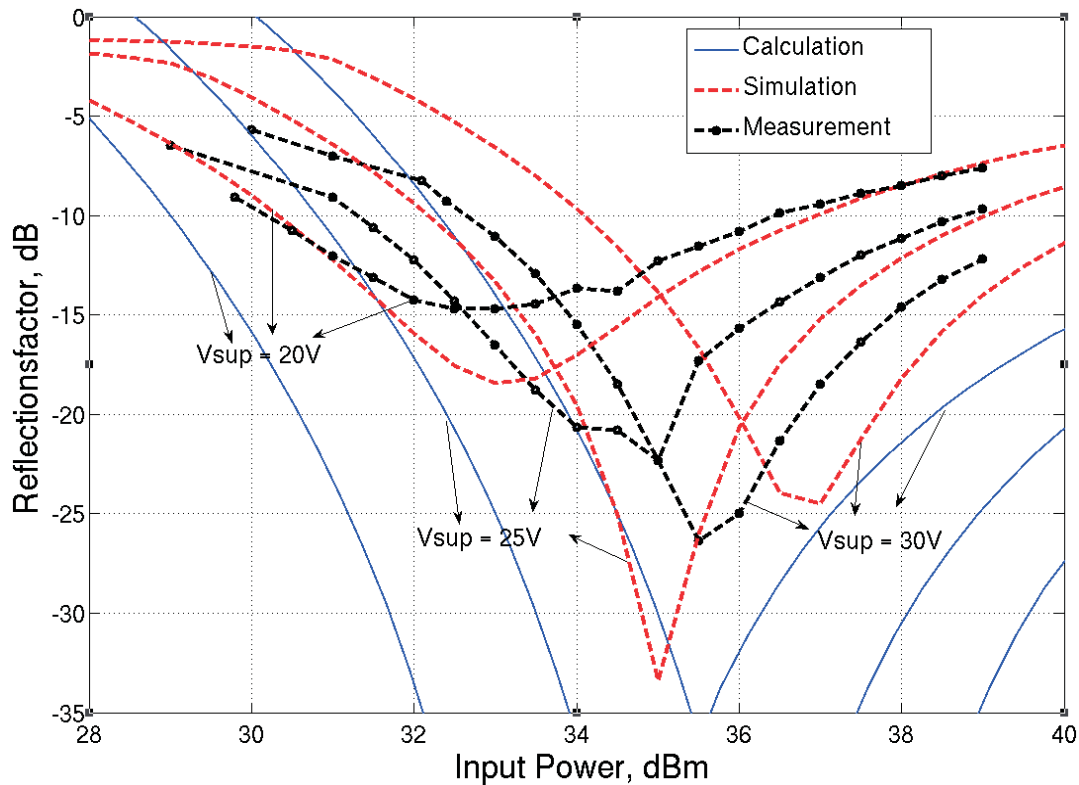
Fig. 9: Comparison of calculated, simulated and measured reflection coefficients as a function of input power level

of the system. With the diode groups, two more recycling circuits were designed. The recycling efficiencies were optimized for an input power level of 36 dBm and 41 dBm, respectively. For all measurements, a peak recycling efficiency of about 60% was achieved. But problems arise due to excesively high currents and voltages at the diodes. The measurement results agree well with the simulations and still show some similarity to the ideal case. This simple technique promises to improve the power efficiency of the outphasing microwave power amplifier, while maintaining its high linearity performance.

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