The Precision Simulation of the First Generation Matrix Converter

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This paper describes simulation of first generation matrix converter, which was realized in the lab. The simulation was developed in response to the need a diagnostic tool. The program is needed in order to debug the implemented control algorithms. The simulator supplies an environment for testing the generation of switching pulses without the risk of damaging the hardware. It supports the large potentiality for quicker development of new switching algorithms. A description of the simulated system is also included.

Keywords: Matrix converter, real-time system, simulation, energy conversion.

1 Introduction

The matrix converter is a system for energy conversion. It is a type of direct frequency converter from the viewpoint of division of power electronics system. The converter is able to control machines supplied with alternate current (asynchronous or synchronous), but it can produce a higher frequency than the best known direct converter – the cycloconverter. A highly sophisticated control algorithm can be implemented to control the machines. This means that from this viewpoint it is comparable with classic indirect frequency converter, but it has many advantages and disadvantage.

The main advantage over the indirect converter is the absence of a DC link and the attendant huge passive elements. As a consequence, a matrix converter can have reduced dimensions. This property can be put to use in space--demanding applications, e.g. traction or flight systems.

Another possible usage of the matrix converter is in connection with medium-frequency transformers.

Other advantages are connected with EMC problems. The power factor of the required energy can be controlled by this type of converter. And finally, it can obtain sinusoidal current from the distribution net.

Like every technical solution, the matrix converter has some disadvantages as every technical solution. These include the large number of semiconductors elements, which need protection from destruction. It is also sensitive to fluctuations in the input voltage.

2 Description of the real system

A description of the realized system is necessary for understanding the simulation parameters. The following description is of the first generation matrix converter realized at the Department of Electric Drives and Traction. Fig. 1 shows the real system configuration. The matrix converter supplies a three-phase squirrel cage asynchronous machine. The DC machine is used as a load. This machine is supplied with four-quadrant DC converter. The system is equipped with a speed sensor.

2.1 Power electronic configuration

The basic element of the matrix converter is a bidirectional switch. A possible bidirectional switch configuration is shown in Fig. 2.

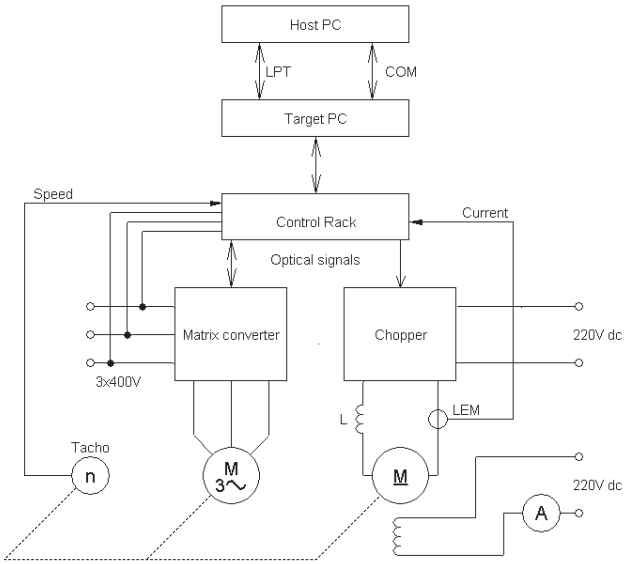

Fig. 1: Configuration of the real system

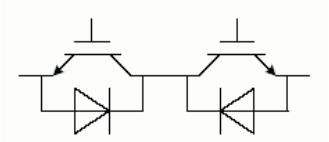

Fig. 2: Bidirectional switch configuration

Configuration of the enlarged compact matrix converter is typically 3×3 switching patterns of 18 IGBTs, as shown in Fig. 3. The compact Eupec IGBT modules FS150R17KE3 are used. The configuration of these modules is adapted to be employed in the matrix converter system. Each module contains 3 bidirectional switches. All the system parts are

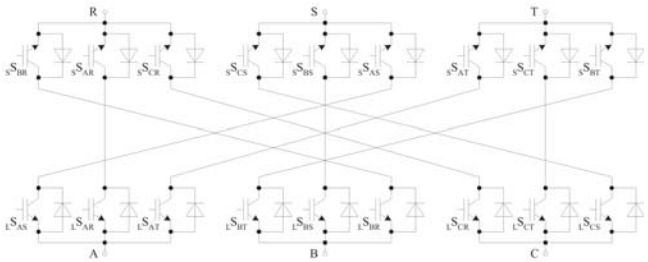

Fig. 3 Switching patterns of the 18 IGBTs

dimensioned for a permanent current stress of 30 A and for a voltage level of 400 V.

2.2 The Control System

The whole system is adapted to comply with the requirement for time precision pulse generation, contemporary control algorithm execution and communication with the user. Two independent personal computers (called Target PC and Host PC) are used to serve these tasks. A specially-designed rack with a controller card is used to generate 18 control pulses. The card is based on the FPGA circuit. A description of FPGA inside the structure is important for simulation quality.

2.2.1 The host PC

The host PC is the nearest part of the converter to the user. It looks like an ordinary PC and it hosts the monitor interface application, which enables the parameters of the converter to be set up. The parameters are given to the second PC through the LPT and COM interface.

2.2.2 The target PC

The execution of the control algorithm is the highest-priority task of this computer. The computer works in hard real-time mode. All system interrupts are disabled. The only way to change the program parameters is through the host PC.

2.2.3 The control rack

The rack is a box which contains control and measurement cards, connected to the system bus, which goes through the rack and the target PC.

Pulse Generation

Two identical cards are used for pulse generation purposes. The first is called the master, and the second is the slave. Each card has 12 optical outputs, which represent one switching word in the regulation program. One FPGA circuit is located on each card. It is programmed similarly as high speed output circuits on some digital signal processors. Each FPGA circuit is able to generate 16 switching words during the regulation period 150 μs in length. The internal structure of FPGA is shown at Fig. 4.

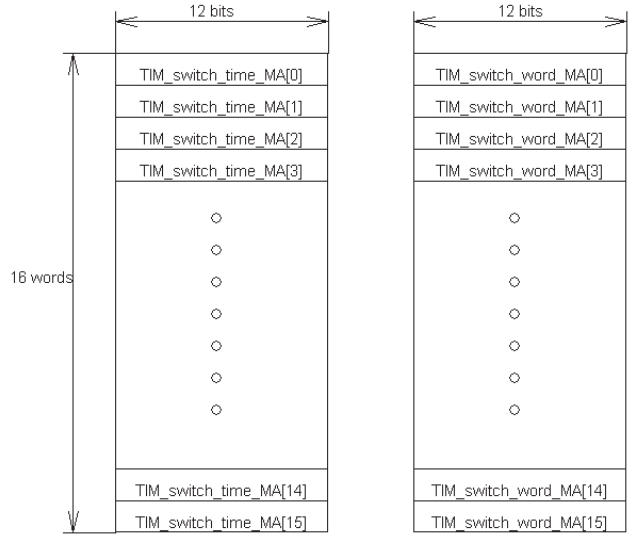

Fig. 4: FPGA structure

16 switching words (called TIM_switch_word) are organized in the table. 16 switching times (in the range between 0 and 150 μs) are assigned to them. The internal timer value is compared to the time value in the table. The corresponding switching word is generated. This switching word stays on the output until it is changed by another word. Not all 16 switching times have to be used in each period. The number of used switching word is called TIM_switch_used. All possible states have been analyzed and reflected upon for simulation purposes.

The other things for simulation are system feedback inputs. Six analog channels are converted to digital information. These must be taken into account in the simulation design.

Program timing

Several operations must be executed in parallel during program execution. It is absolutely necessary take into consideration real system timing during simulation design. The timing of the simulation and the real system must be identical. Otherwise the simulation will lost its seriousness. The system timing is shown in Fig. 5.

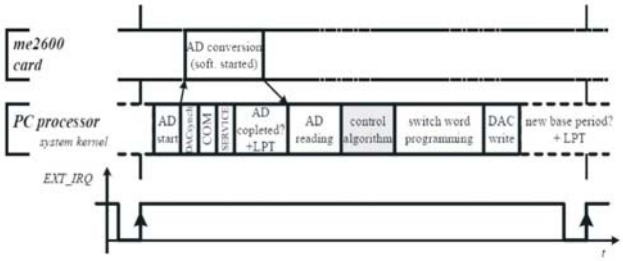

Fig. 5: System timing

The main program loop takes a time of 150 μs. That means a switching frequency of the power transistors of about 6.6 kHz. The internal timer step is 1/20. 1/20 μs is the basic time unit for the whole system. One program loop takes 3000 of basic time units. Therefore 12-bit wide time information is needed in the switching table.

2.2.4 The control software

The Target PC's software includes the whole firmware for initialization, the AD conversion service, communication and, of course, the application program. The application program is the most important for simulation purposes. It is necessary to take care about the full compatibility and portability of the source code between the simulation and the real system. Basic modules and strict rules had to be settled.

3 The simulation

3.1 The requirements

The most important requirement is source code compatibility between the simulation and the real system. The simulation must return an adequate response to enable software debugging and error finding. The adequate response must be ensured not only for the correct algorithm, but also for error states.

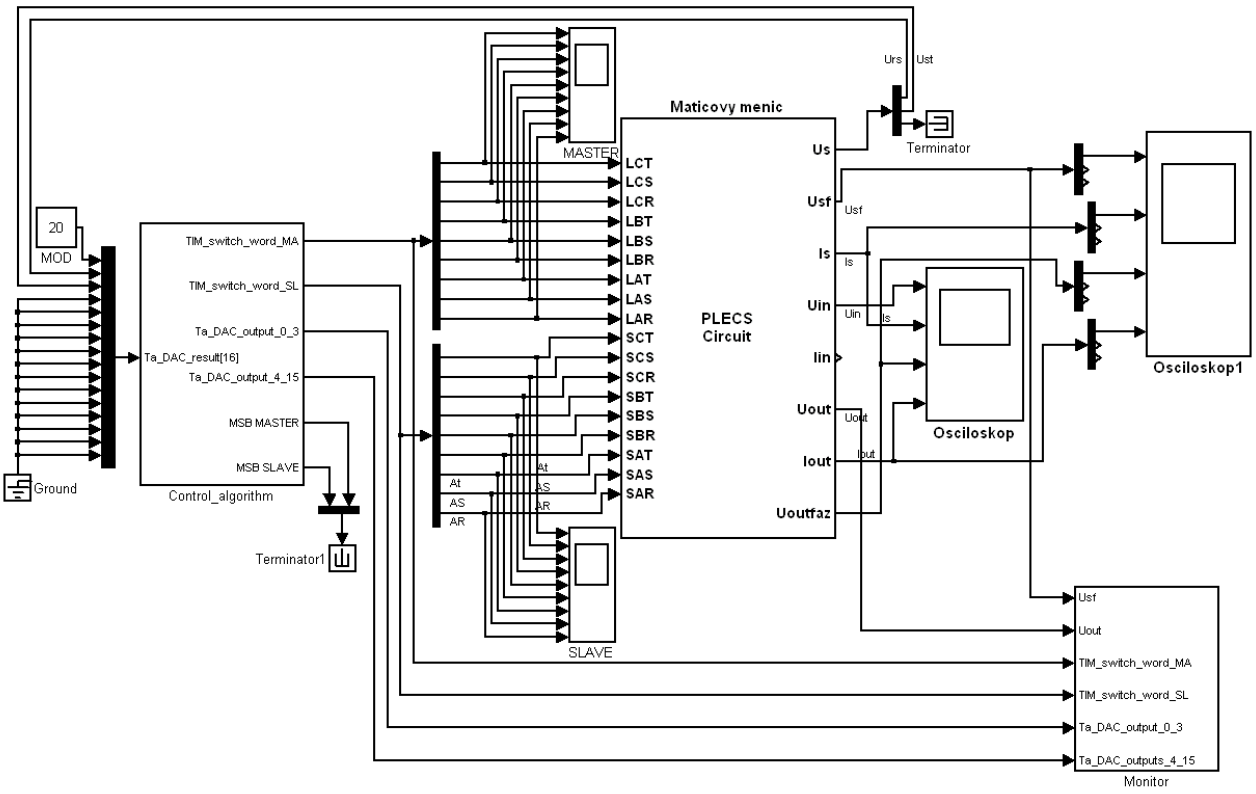

Fig. 6: The whole model view. The basic blocks are shown in this picture. The main control block is on the left. The switching pulses are on the output. These pulses are monitored by the scope blocks, by the auto error detection block, which can be seen in the bottom right corner (called the Monitor). This inputs into the Plecs block located in the middle part of the figure. The monitoring block is on the right, where the electrical magnitudes are shown.

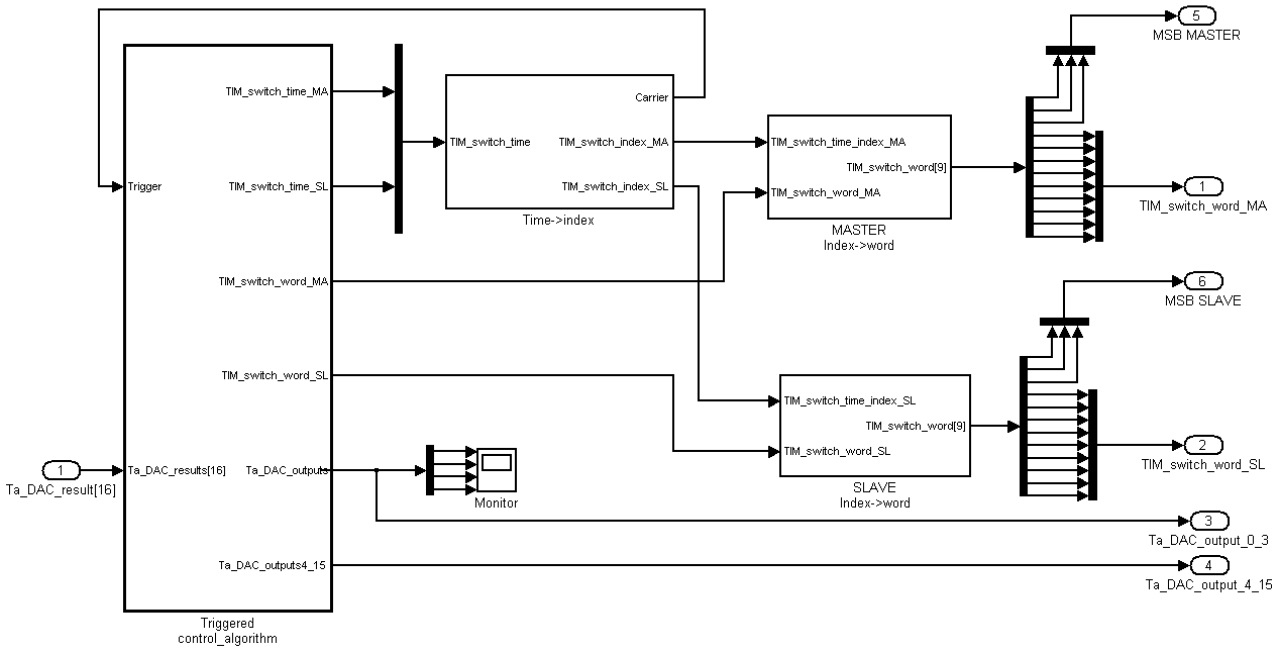

Fig. 7: The interface between the real system and the portable simulation program and pulse generation. An operation which has to be applied to the output of the real program block situated on left side. The block called Time→index is very important for time synchronization of the whole model.

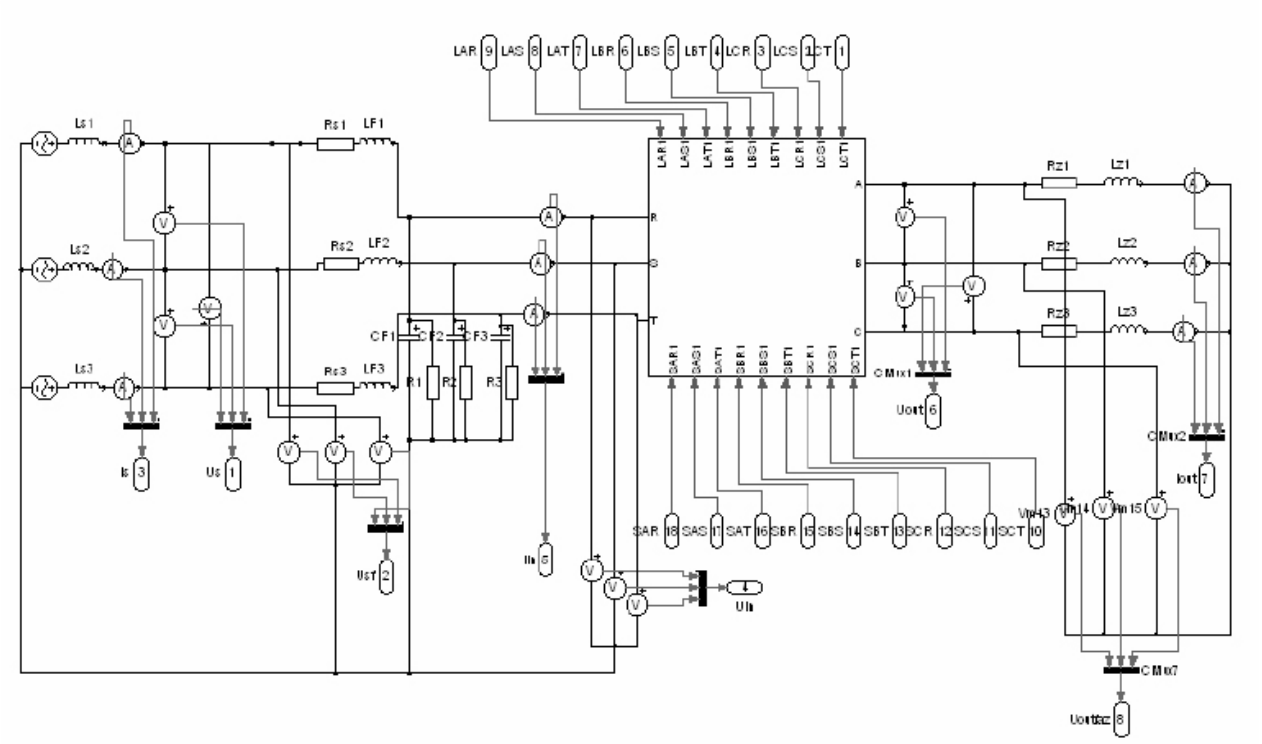

Fig. 8: The power part simulation block in Plecs

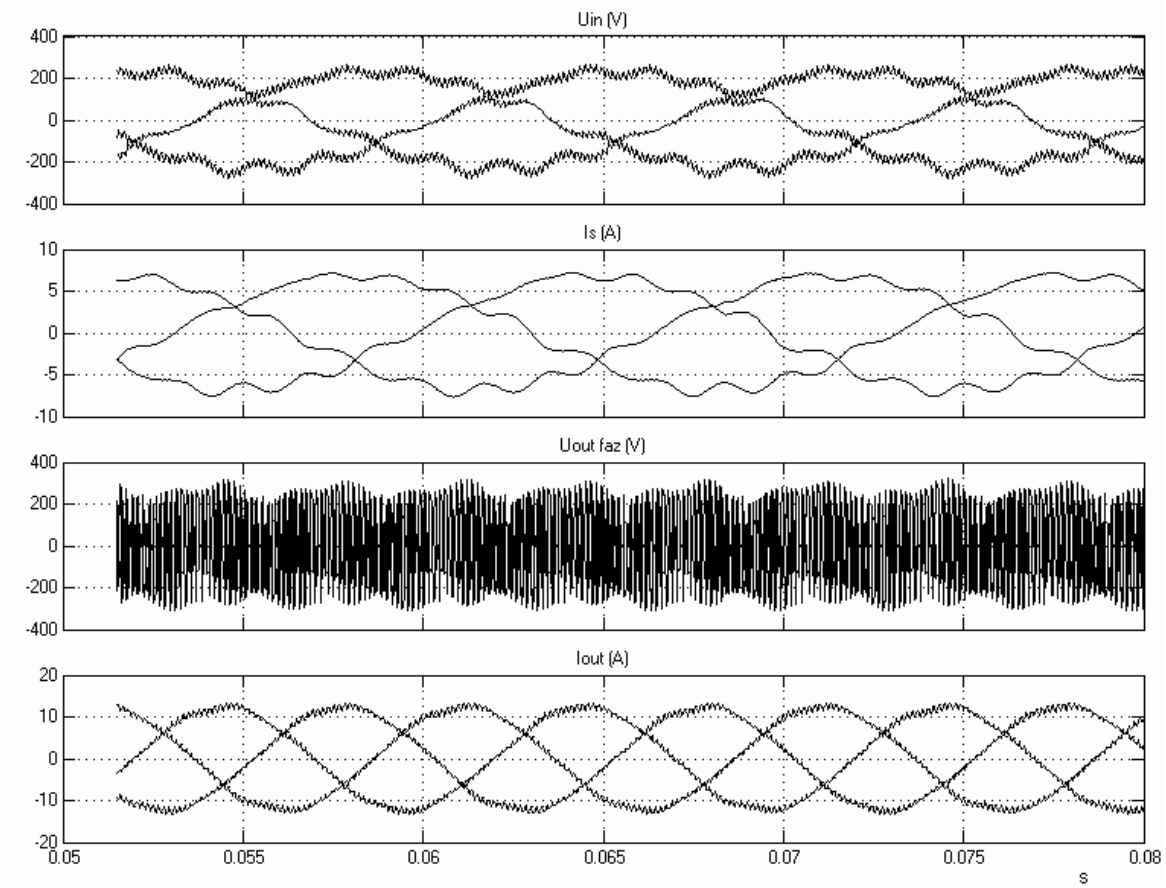

Fig. 9: Simulation outputs. Some examples of the simulation result are shown here. The first and second graphs show input magnitudes (voltage and current). The third and fourth graphs show output voltage and current. This figure shows the input filter oscillation.

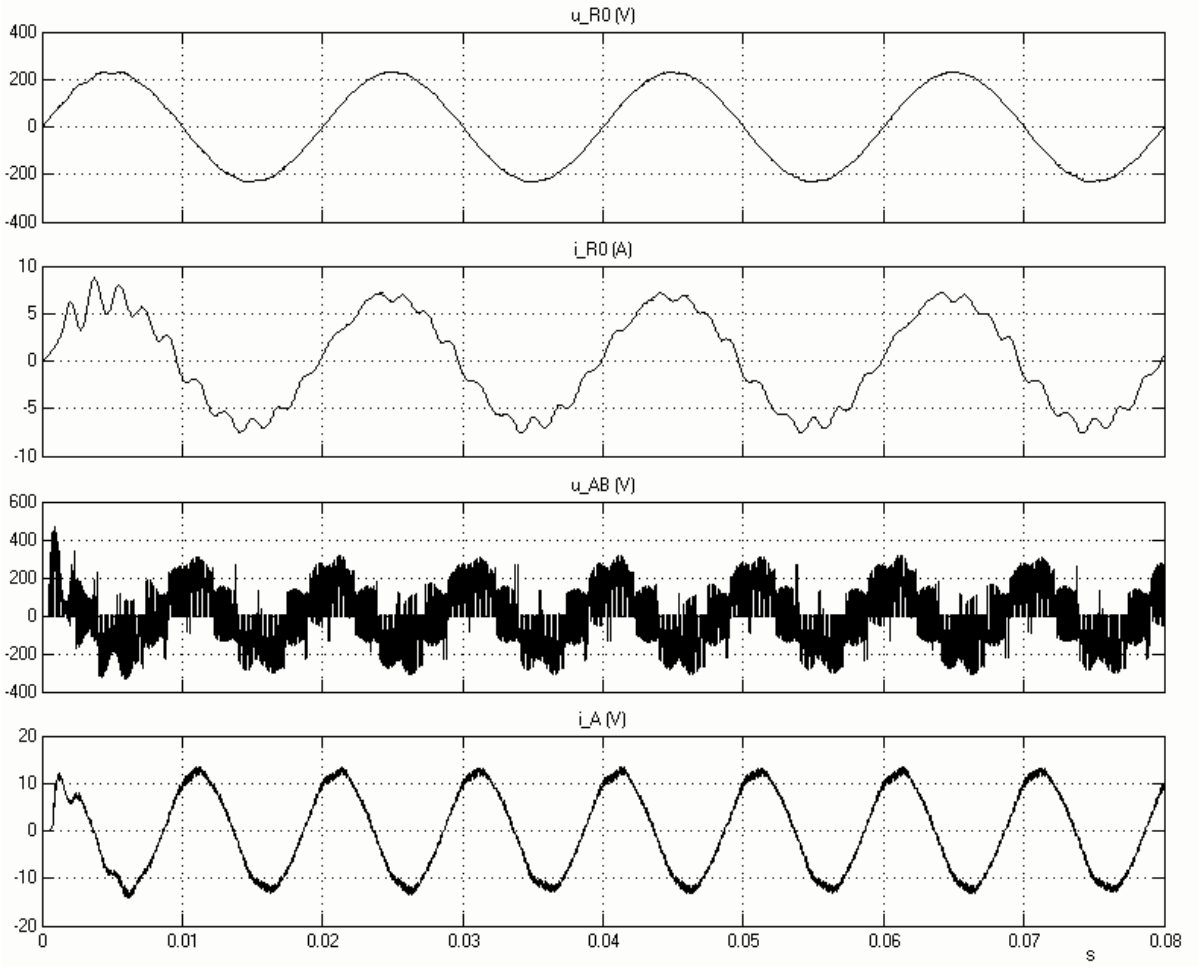

Fig. 10 The one-phase simulation result. Input voltage, input current, output voltage, output current

The simulation must be optimized from the viewpoint of time consumption.

Automatic error state identification is required. It will be useful, if the simulation can identify switching word errors that can damage the real system.

3.2 The environment

The simulation has been developed for the Matlab Simulink environment, and the Plecs module simulating electric circuits has been used. The source code is written in C language.

It can be seen that there are two different levels. The first one is the model of the lab. The second level includes the environment for source code transfer between the real system and simulation. An interface between the source code and Matlab has been developed. The MEX function system provided by Matlab has been used. Another possible interface, called S-function, was rejected because of its slow response.

The model configuration is shown in Figs. 6–8.

4 Results

Many simulations have been made and some useful results have been obtained. Some control algorithms have been tested (four step commutation, two step commutation, over-modulation) and some of the experience that has been acquired has been used in developing the second generation matrix converters.

References

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