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New Electronically Tunable Third Order Filters and Dual Mode Sinusoidal Oscillator Using VDTAs and Grounded Capacitors

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Abstract

This study introduces a third order filter and a third order oscillator configuration. Both the circuits use two voltage difference transconductance amplifiers (VDTAs) and three grounded capacitors. By selecting the input and output terminals properly, current mode and transimpedance mode low-pass and band-pass filters can be obtained without component matching conditions. The natural frequency (ω_0) can be tuned electronically. The oscillator circuit provides voltage and current outputs explicitly. The condition of oscillation (CO) and the frequency of oscillation (FO) can be adjusted orthogonally and electronically. The workability of the configurations is judged using TSMC CMOS 0.18 μm technology parameter as well as commercially available LM13700 integrated circuits (ICs). The simulation results show that: for ±0.9V power supply, the power consumption is 1.08 mW for both the configurations, while total harmonic distortions (THDs) are less than 2.06% and 2.17% for the filter and oscillator configurations, respectively.

Keywords: dual mode third order oscillator, third order filter, total harmonic distortion (THD), voltage difference transconductance amplifier (VDTA)

1. Introduction

Although there has been a great development in the field of digital signal processing, the devices which are entirely capable of processing analog signals have not lost their popularity because all the natural signals are analog in nature. Analog signal processing (ASP), in which natural/analog signals are handled according to the specifications, has advantages such as higher bandwidth, faster operation speed, etc. Filter and sinusoidal oscillators are two widely used applications in the field of ASP [1].

Filters are very useful for signal processing circuits in instrumentation, control engineering, and various communication systems. Filters are also useful in phase shifting, frequency doubling, and interfacing with other circuits. Current mode filters offer some advantages, e.g., low power consumption, wide bandwidth, wider dynamic range, and high slew rate [1]. Third order filters have a sharper cut-off than biquadratic filters, which is a great advantage in various communication applications. Recently, there has been an increasing interest in designing a filter employing various active building blocks (ABBs) such as four terminal floating nullor (FTFN) [2], voltage differencing buffered amplifier (VDBA) [3], differential difference current conveyor (DDCC) [4], current differencing buffered amplifier (CDBA) [5], differential voltage current conveyor (DVCC) [6], voltage differencing current conveyor (VDCC) [7], voltage differencing transconductance amplifier (VDTA) [8], etc. Most of the reported circuits are second-order filters [1-8]. However, some research also deal with third order and higher order filters [9-25]. These filters suffer from one or more of the following drawbacks:

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(1) More than two ABBs are used [4, 10-11, 16-21, 23, 25].

(2) Comparatively large supply voltage is required [2-3, 8, 10-14, 18, 23-25].

(3) Circuits are not resistorless [1-2, 4-6, 7, 9, 12-16, 22-24].

(4) All the used capacitors are not grounded [2-3, 5-6, 12-15, 24-25].

(5) Double/inverted input signals are required for response realization [2-3, 5-6, 25].

(6) Matching conditions are required to realize various filter responses [6, 9, 11, 13, 15, 24].

(7) The natural frequency is not electronically tunable [2, 4-6, 9-10, 12-17, 21-24].

Sinusoidal oscillators play a vital role in power electronics, measurement, standard tests, communication systems, and instrumentation. The third order sinusoidal oscillators offer better frequency response and low harmonic distortion than second order oscillators [26]. Recently, a number of oscillators using VDTA as an active block have already been published [26-29], but all the reported circuits have one or more limitations:

(1) The oscillators require additional terminals for VDTA blocks [26-29].

(2) Matching condition is required [26].

A universal current mode biquad filter is proposed in the work of Satansup et al. [8]. The topology of their work has become our topic of contemplation. We have considered carefully appending a VDTA block and a capacitor to realize third order low-pass (LP) and band-pass (BP) filters. By making slight changes to the filter configuration, a third order sinusoidal oscillator can also be realized.

Thus, the aim of this work is to propose a third order filter and a dual mode third order oscillator configuration employing two VDTAs and three grounded capacitors without the use of any resistors. The features of the proposed filters are that: (i) the configuration uses two active components and three grounded capacitors; (ii) the natural frequency can be tuned electronically; (iii) double/inverted input signals are not required for response realizations; (iv) the proposed filters use only grounded capacitors; (v) matching conditions are not required to realize various filter responses; (vi) the proposed filters have low active and passive sensitivities. The proposed third-order quadrature oscillator has the following advantages simultaneously: (i) like third order filter, it contains only two active components and three grounded capacitors; (ii) it provides explicit current output; (iii) it has a voltage mode and a current mode sinusoidal output; (iv) it has orthogonally and electronically tunable characteristics for the condition of oscillation (CO) and the frequency of oscillation (FO); (v) it uses only grounded capacitors; (vi) it has low active and passive sensitivity. The workability of the proposed configurations is verified using the TSMC CMOS 0.18 μm technology parameter as well as commercially available LM13700 integrated circuits (ICs). Both the theoretical and personal simulation program with integrated circuit emphasis (PSPICE) simulated results are depicted in the frequency response graph.

The manuscript is divided into nine sections, including this one. The basic concept of the VDTA block is described in section 2. Section 3 presents the proposed configurations. In section 4, the non-ideality effects of VDTA is described, followed by section 5 where the sensitivity analysis is described. The simulation and experimental results are thoroughly explained in section 6 and section 7, respectively. Furthermore, in section 8, the comparison of the proposed work with the available literature is discussed. The manuscript is concluded in section 9.

2. Basic Concept of VDTA

VDTA is a current mode ABB. The circuit symbol and inner block diagram of VDTA are shown in Fig. 1, where P and N are the input ports and Z, X+, and X− are the output ports. All ports show high impedance values [26]. In VDTA, the difference between two input voltages is transferred to current at the Z port by first transconductance gain (g_{mF}). The voltage drop at the Z port is transferred to current at the X port by second transconductance gain (g_{mS}). Both transconductances can be controlled electronically by external bias currents. The port relations of an ideal VDTA can be expressed as [8]:

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ I_X \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{mF} & -g_{mF} & 0 & 0 \\ 0 & 0 & 0 & g_{mS} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_X \\ V_Z \end{bmatrix} \tag{1}$$

The complementary metal oxide semiconductor (CMOS) implementation of VDTA, which consists of two Arbel-Goldminz transconductances, is depicted in Fig. 2 [30]. The two electronically tunable transconductances g_{mF} and g_{mS} of VDTA can be expressed as:

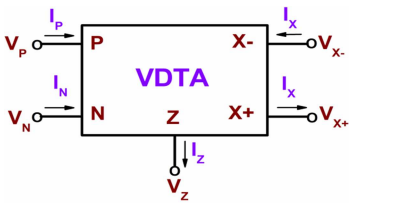
$$g_{mF} = \frac{(g_{m1} + g_{m5})}{2} \; or \; g_{mF} = \frac{(g_{m2} + g_{m6})}{2} \tag{2}$$

$$g_{mS} = \frac{(g_{m3} + g_{m7})}{2} \; or \; g_{mS} = \frac{(g_{m4} + g_{m8})}{2} \tag{3}$$

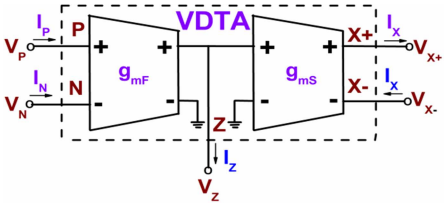
The value of transconductance can be expressed as:

$$g_{mi} = \sqrt{I_{Bi} C_{ox} \mu_i (\frac{w}{L})_i} \tag{4}$$

where I_{Bi} is the bias current of i-th transistor, C_{ox} is the gate-oxide capacitance per unit area, μ_i is the carrier mobility for p-channel metal oxide semiconductor (PMOS) or n-channel metal oxide semiconductor (NMOS) transistors, w is the effective channel width, and L is the length of the i-th transistor (i = 1, 2,…, 8), respectively.



(a) Symbolic representation



(b) Inner block diagram

Fig. 1 VDTA [8]

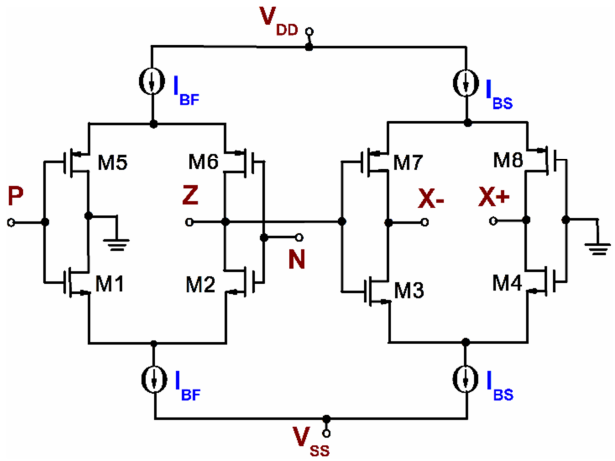


Fig. 2 The CMOS based internal circuit construction of VDTA [30]

3. The Proposed Configurations

3.1. The proposed third order filter circuit

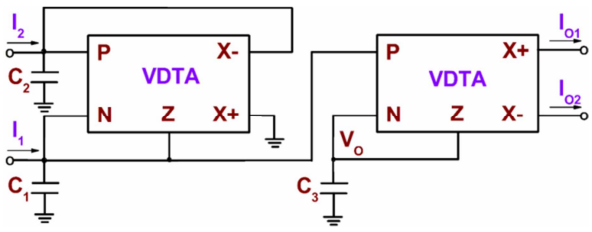


Fig. 3 The proposed resistorless and electronically tunable third order filter

The proposed third order current mode and transimpedance mode filter configuration consisting of two VDTA blocks and three grounded capacitors is shown in Fig. 3. The routine analysis of this filter circuit yields the output currents and voltage as:

$$I_{O1} = -I_{O2} = \frac{s\frac{g_{mF2}g_{mS2}}{C_1C_3}I_1 + \frac{g_{mF1}g_{mF2}g_{mS2}}{C_1C_2C_3}I_2}{D(s)} \tag{5}$$

$$V_O = \frac{s\frac{g_{mF2}}{C_1C_3}I_1 + \frac{g_{mF1}g_{mF2}}{C_1C_2C_3}I_2}{D(s)} \tag{6}$$

where g_{mF1} is the first transconductance gain of VDTA1, g_{mS1} is the second transconductance gain of VDTA1, g_{mF2} is the first transconductance gain of VDTA2, g_{mS2} is the second transconductance gain of VDTA2, and $D(s)$ can be expressed as:

$$D(s) = s^3 + s^2\left(\frac{g_{mF1}}{C_1} + \frac{g_{mF2}}{C_3}\right) + s\frac{g_{mF1}}{C_1}\left(\frac{g_{mF2}}{C_3} + \frac{g_{mS1}}{C_2}\right) + \frac{g_{mF1}g_{mF2}g_{mS1}}{C_1C_2C_3} \tag{7}$$

Thus, the reported filter configuration can realize current mode (inverting and non-inverting) and transimpedance mode (non-inverting) LP and BP third order filters. Eqs. (5)-(6) have two input sections that allow the designer to select the appropriate inputs for achieving filter responses. The selection of input and output terminals for realizing the current mode and transimpedance mode filter responses is shown in Table 1. The performance parameters of the filters, namely, natural frequency (ω_0) and quality factor (Q) can be calculated according to the Akerberg-Mossberg approximation [25] by putting $s^3 = -s\omega^2$ in $D(s)$. The calculated natural frequency and quality factor can be written as:

$$\omega_0 = \sqrt{\frac{g_{mF1}g_{mF2}g_{mS1}}{C_2(C_3g_{mF1} + C_1g_{mF2})}} \tag{8}$$

$$Q = \frac{\sqrt{g_{mF1}g_{mF2}g_{mS1}C_2(C_3g_{mF1} + C_1g_{mF2})^3}}{g_{mF1}[C_3g_{mF1}(C_2g_{mF2} + C_3g_{mS1}) + C_1C_2g_{mF2}^2]} \tag{9}$$

If $C_1 = C_2 = C_3 = C$ and $g_{mF1} = g_{mF2} = g_{mS1} = g_{mS2} = g_m$, then $Q = 0.942$ and the expression of ω_0 becomes:

$$\omega_0 = \frac{g_m}{\sqrt{2}C} \tag{10}$$

Table 1 Selection of input and output terminals for realizing different filter functions

Filter responses	Input		Output (I_{O1} or I_{O2} or V_O)
	I_1	I_2	
LP1 (non-inverting current mode)	0	I_{in}	I_{O1}
LP2 (inverting current mode)	0	I_{in}	I_{O2}
LP3 (non-inverting transimpedance mode)	0	I_{in}	V_O
BP1 (non-inverting current mode)	I_{in}	0	I_{O1}
BP2 (inverting current mode)	I_{in}	0	I_{O2}
BP3 (non-inverting transimpedance mode)	I_{in}	0	V_O

3.2. The proposed third order dual mode sinusoidal oscillator circuit

By making minor modifications to the proposed third order filter configuration, a dual mode third order sinusoidal oscillator circuit which is depicted in Fig. 4 can be realized. The reported oscillator circuit provides explicit current and voltage

outputs. The theoretical analysis of the oscillator circuit yields the characteristic equation as shown in Eq. (11). Based on Eq. (11), the reported third order oscillator can generate oscillation in the case that the oscillation condition shown in Eq. (12) is fulfilled. The oscillation frequency is expressed in Eq. (13).

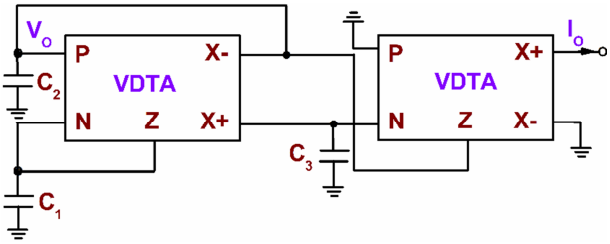


Fig. 4 The proposed resistorless and electronically tunable third order oscillator

$$s^3 + s^2\frac{g_{mF1}}{C_1} + s\frac{g_{mF1}g_{mS1}}{C_1C_2} + \frac{g_{mF1}g_{mF2}g_{mS1}}{C_1C_2C_3} = 0 \tag{11}$$

$$\text{CO: } C_3g_{mF1} = C_1g_{mF2} \tag{12}$$

$$\text{FO: } \omega_0 = \sqrt{\frac{g_{mF2}g_{mS1}}{C_2C_3}} \tag{13}$$

Eqs. (12)-(13) confirm that CO and FO can be adjusted orthogonally. For example, CO can be adjusted by g_{mF1} without disturbing FO, and FO can be adjusted by g_{mS1} without hampering CO. Both the transconductance gains, g_{mF1} and g_{mS1} of the VDTA, can be tuned electronically by the two bias currents I_{BF1} and I_{BS1} respectively. I_{BFK} and I_{BSK} are the bias currents, I_{BF} and I_{BS} of the k-th VDTA (k = 1, 2). Thus, the CO and FO of the derived third order sinusoidal oscillator can be adjusted orthogonally by two bias currents I_{BF1} and I_{BS1} respectively.

4. Non-Ideality Effects of VDTA

The non-ideality effects of VDTA have been discussed in this section. In practice, these non-idealities are classified as tracking errors and parasitics. The non-ideality arises due to an error in the transconductance transfer function from P and N terminals to Z terminals and Z terminals to X terminals. The terminal relationships of VDTA including tracking errors of the VDTA can be rewritten as: $I_Z = \beta_{Fi}g_{mFi}(V_P - V_N)$ and $I_X = \beta_{Si}g_{mSi}V_Z$. β_{Fi} and β_{Si} are the tracking errors of i-th VDTA [8].

In addition, like any other active device, a practical VDTA shows various terminals parasitics. At all terminals, VDTA has a high parasitic resistance in parallel with low valued parasitic capacitance. The parasites in the form of shunt output impedances (R_P//C_P), (R_N//C_N), (R_Z//C_Z), (R_{X+}//C_{X+}), and (R_{X-}//C_{X-}) appear at P, N, Z, X+, and X− ports respectively. The non-ideal model of VDTA is shown in Fig. 5.

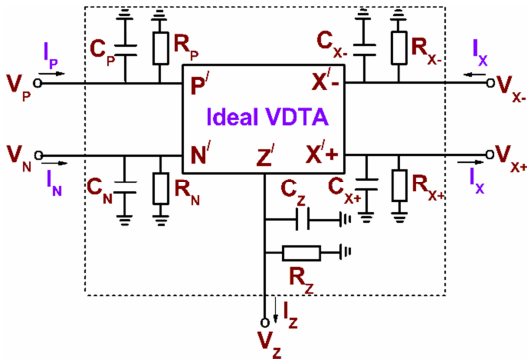


Fig. 5 Non-ideal VDTA showing its parasitic impedances [8]

4.1. Non-ideal analysis of the proposed third order filter

Considering these parasitics in the proposed filter, Fig. 3 is modified to Fig. 6. The components including the influence of parasites are simplified as follows:

$$C_{E1} = C_1 + C_{Z1} + C_{N1} + C_{P2} \tag{14}$$

$$C_{E2} = C_2 + C_{P1} + C_{X1-} \tag{15}$$

$$C_{E3} = C_3 + C_{Z2} + C_{N2} \tag{16}$$

$$R_{E1} = R_{P2} \parallel R_{N1} \parallel R_{Z1} \tag{17}$$

$$R_{E2} = R_{P1} \parallel R_{X1-} \tag{18}$$

$$R_{E3} = R_{N2} \parallel R_{Z2} \tag{19}$$

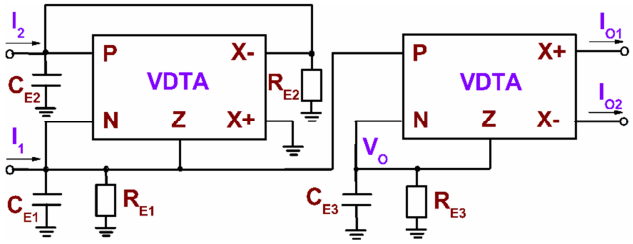


Fig. 6 The proposed resistorless and electronically tunable third order filter with device parasitics

Considering the above non-ideality and parasitics, the natural frequency and quality factor are given by Eq. (20) and Eq. (21), respectively.

$$\omega_0^{'} = \sqrt{\frac{d}{b}} \tag{20}$$

$$Q^{'} = \frac{\sqrt{b^3 d}}{bc - ad} \tag{21}$$

where

$$a = C_{E1} C_{E2} C_{E3} \tag{22}$$

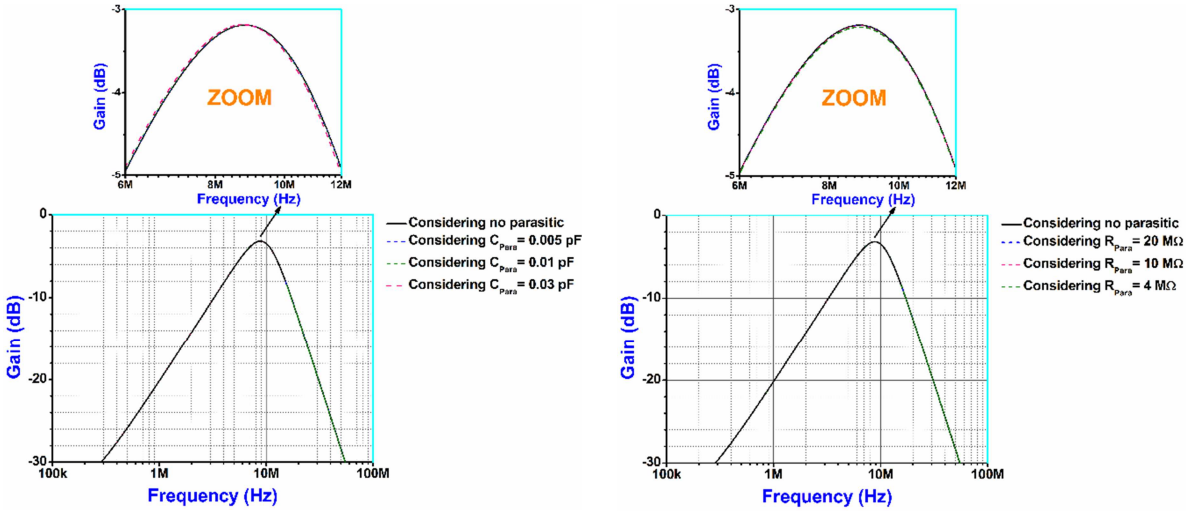
$$b = C_{E2}\left(\beta_{F1} C_{E3} g_{mF1} + \beta_{F2} C_{E1} g_{mF2}\right) + \left(\frac{C_{E2} C_{E3}}{R_{E1}} + \frac{C_{E1} C_{E3}}{R_{E2}} + \frac{C_{E1} C_{E2}}{R_{E3}}\right) \tag{23}$$

$$c = \beta_{F1} g_{mF1}(\beta_{F2} C_{E2} g_{mF2} + \beta_{S1} C_{E3} g_{mS1}) + \left(\begin{array}{l} \frac{\beta_{F2} C_{E2} g_{mF2}}{R_{E1}} + \frac{\beta_{F1} C_{E2} g_{mF1}}{R_{E2}} + \frac{\beta_{F2} C_{E1} g_{mF2}}{R_{E3}} + \frac{C_{E1}}{R_{E2} R_{E3}} + \frac{C_{E2}}{R_{E1} R_{E3}} \\ + \frac{C_{E3}}{R_{E1} R_{E2}} + \frac{\beta_{F1} \beta_{S1} C_{E3} g_{mF1} g_{mS1}}{R_{E1} R_{E2} R_{E3}} \end{array}\right) \tag{24}$$

$$d = \beta_{F1} \beta_{F2} \beta_{S1} g_{mF1} g_{mF2} g_{mS1} + \left(\frac{\beta_{F1} \beta_{F2} g_{mF1} g_{mF2}}{R_{E2}} + \frac{\beta_{F1} \beta_{S1} g_{mF1} g_{mS1}}{R_{E3}} + \frac{\beta_{F1} g_{mF1}}{R_{E2} R_{E3}} + \frac{\beta_{F2} g_{mF2}}{R_{E1} R_{E2}} + \frac{1}{R_{E1} R_{E2} R_{E3}}\right) \tag{25}$$

It is seen from Eqs. (20)-(21) that the natural frequency and quality factor have been slightly changed due to the non-ideality errors of VDTA. In reality, the effect can be observed in the simulation curves where a small deviation will appear when compared to theoretical graphs. From the above expressions, it is also observed that ω_0 and Q are affected due to the parasitic of VDTA, but it is not adverse as the values of parasitic resistances are very high in comparison to transconductance gains. Furthermore, the values of parasitic capacitances are very low compared to external capacitors. As a result, $C_{E1} = C_1$, $C_{E2} = C_2$, and $C_{E3} = C_3$. By assuming these values of capacitors and neglecting the terms which are associated with parasitic resistances, Eq. (20) and Eq. (21) can be approximated to the ideal value of ω_0 and Q. Therefore, it may be concluded that, by choosing external capacitances much higher than parasitic capacitances, the output frequency response of the reported circuit would not be affected.

Adding some sample values of parasitic capacitors ($C_{P1} = C_{P2} = C_{N1} = C_{N2} = C_{Z1} = C_{Z2} = C_{X1+} = C_{X2+} = C_{X1-} = C_{X2-} = C_{Para}$) and resistors ($R_{P1} = R_{P2} = R_{N1} = R_{N2} = R_{Z1} = R_{Z2} = R_{X1+} = R_{X2+} = R_{X1-} = R_{X2-} = R_{Para}$) at all the terminals of VDTA, the parasitic influence on the current mode BP filter (BP1) is shown in Fig. 7. Fig. 7(a) indicates that the proposed filter circuit would not be affected by up to 0.03 pF parasitic capacitances. At 10 MΩ parasitic resistance, a small deviation is noticeable in Fig. 7(b). Therefore, the performance of the proposed filter cannot be affected above the 10 MΩ parasitic resistance.



(a) For parasitic capacitors (b) For parasitic resistors

Fig. 7 Parasitic influence on the performance of the proposed BP1 filter

4.2. Non-ideal analysis of the proposed third order sinusoidal oscillator

Considering the parasitics in the proposed sinusoidal oscillator, Fig. 4 is modified to Fig. 8. The components are simplified as follows:

$$C_{E1} = C_1 + C_{Z1} + C_{N1} \tag{26}$$

$$C_{E2} = C_2 + C_{P1} + C_{X1-} + C_{Z2} \tag{27}$$

$$C_{E3} = C_3 + C_{X1+} + C_{N2} \tag{28}$$

$$R_{E1} = R_{Z1} \parallel R_{N1} \tag{29}$$

$$R_{E2} = R_{P1} \parallel R_{X1-} \parallel R_{Z2} \tag{30}$$

$$R_{E3} = R_{X1+} \parallel R_{N2} \tag{31}$$

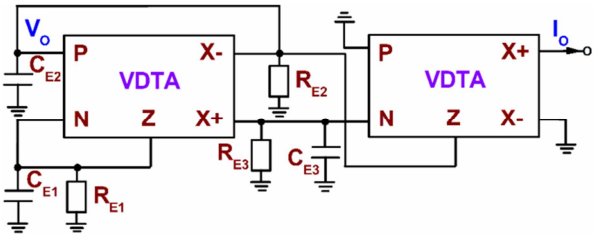


Fig. 8 The proposed resistorless and electronically tunable third order oscillator with device parasitics

Using non-ideality errors and parasitic model of VDTA, the characteristic equation changes to:

$$s^3 + s^2 X + sY + Z = 0 \tag{32}$$

where

$$X = \frac{\beta_{F1} g_{mF1}}{C_{E1}} + \left(\frac{1}{C_{E1} R_{E1}} + \frac{1}{C_{E2} R_{E2}} + \frac{1}{C_{E3} R_{E3}} \right) \tag{33}$$

$$Y = \frac{\beta_{F1} \beta_{S1} g_{mF1} g_{mS1}}{C_{E1} C_{E2}} + \frac{\beta_{F1} g_{mF1}}{C_{E1}} \left(\frac{1}{C_{E3} R_{E3}} + \frac{1}{C_{E2} R_{E2}} \right) + \left(\frac{1}{C_{E1} C_{E3} R_{E1} R_{E3}} + \frac{1}{C_{E1} C_{E2} R_{E1} R_{E2}} + \frac{1}{C_{E2} C_{E3} R_{E2} R_{E3}} \right) \tag{34}$$

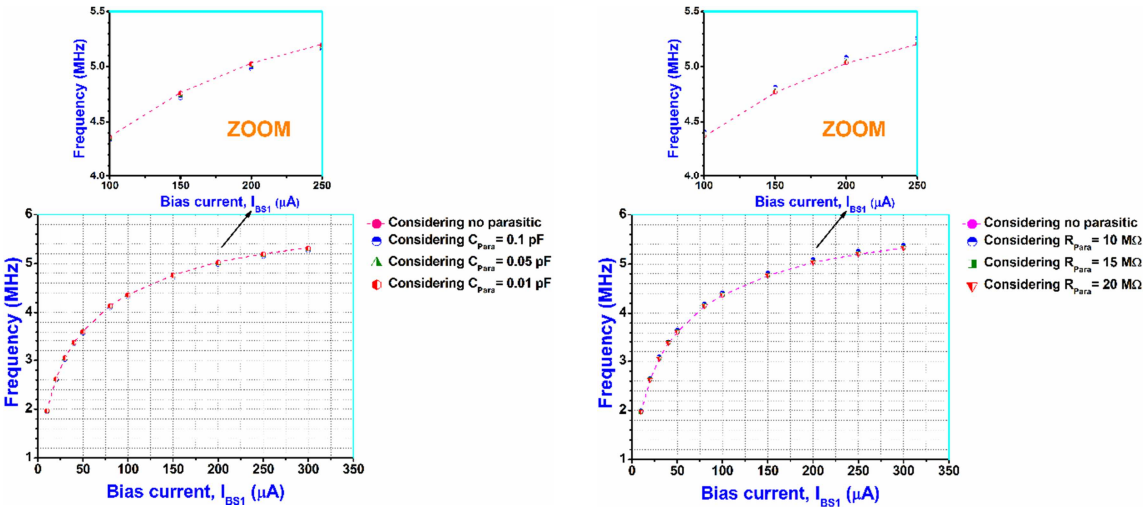
$$Z = \frac{\beta_{F1} \beta_{F2} \beta_{S1} g_{mF1} g_{mF2} g_{mS1}}{C_{E1} C_{E2} C_{E3}} + \frac{1}{C_{E1} C_{E2} C_{E3}} \left(\frac{\beta_{F1} \beta_{S1} g_{mF1} g_{mS1}}{R_{E3}} + \frac{\beta_{F1} g_{mF1}}{R_{E2} R_{E3}} + \frac{1}{R_{E1} R_{E2} R_{E3}} \right) \tag{35}$$

The modified CO and FO are given by:

$$\text{CO: } XY = Z \tag{36}$$

$$\text{FO: } \omega_0' = \sqrt{\frac{Z}{X}} \tag{37}$$

Eqs. (36)-(37) show that CO and FO are slightly deviated due to non-ideality errors, but as the values of non-ideality errors are very near to unity, the deviations are minute. Hence, even when non-ideality errors are considered, the oscillator's performance is close to that of the ideal. Eqs. (36)-(37) also show that CO and FO are affected due to the parasitics of VDTA. The parasitic effect is not noticeable if the values of C_1, C_2, and C_3 are chosen to be large compared to the parasitic capacitors.



(a) For parasitic capacitors (b) For parasitic resistors

Fig. 9 Variation of frequency considering parasitics at different terminals

The parasitic influences on the oscillator are investigated. Considering some sample values of parasitic capacitors and resistors, at all the terminals of the VDTA, the variation in oscillation frequency with regard to bias current is shown in Fig. 9. Fig. 9(a) indicates that the proposed oscillator circuit would not be affected by up to 0.01 pF parasitic capacitances. At 15 MΩ parasitic resistance, a small deviation is noticeable in Fig. 9(b). Therefore, the performance of the proposed oscillator cannot be affected above the 15 MΩ parasitic resistance.

Thus, the limitation is that the values of external capacitors should be chosen much higher than C_{P1}, C_{P2}, C_{N1}, C_{N2}, C_{Z1}, C_{Z2}, C_{X1+}, C_{X2+}, C_{X1-}, and C_{X2-} to ignore the parasitic effects easily. To satisfy these conditions, the circuits may be realized using external capacitors instead of using on chip capacitors.

5. Sensitivity Analysis

The practical solution is to design a network that has low sensitivity to element changes. Thus, sensitivity must be less than the limit, i.e., unity. The lower the sensitivity of the circuit is, the less its performance deviate will be because of element changes [19]. The sensitivity of frequency (ω_0) regarding circuit parameter X (say) is expressed as [31]:

$$S_X^{\omega_0} = \frac{X}{\omega_0}\frac{\partial \omega_0}{\partial X} \tag{38}$$

5.1. Sensitivity analysis of the proposed filter

Using the above definition, the sensitivities of ω_0 for the filter circuit with regard to active and passive components are obtained as:

$$\left.\begin{aligned} S_{g_{mF1}}^{\omega_0} &= -S_{C_1}^{\omega_0} = \frac{C_1 g_{mF2}}{2(C_3 g_{mF1} + C_1 g_{mF2})} \\ S_{g_{mF2}}^{\omega_0} &= -S_{C_3}^{\omega_0} = \frac{C_3 g_{mF1}}{2(C_3 g_{mF1} + C_1 g_{mF2})} \\ S_{g_{mS1}}^{\omega_0} &= -S_{C_2}^{\omega_0} = \frac{1}{2} \\ S_{g_{mS2}}^{\omega_0} &= 0 \end{aligned}\right\} \tag{39}$$

It is seen from Eq. (39) that all of the passive sensitivities are not more than 1/2 in magnitude. Thus, it confirms that the sensitivity performance is satisfactory.

5.2. Sensitivity analysis of the proposed oscillator

From Eq. (12), the value of g_{mF2} can be expressed as:

$$g_{mF2} = \frac{C_3 g_{mF1}}{C_1} \tag{40}$$

Putting this value of g_{mF2} in Eq. (13), the value of ω_0 can be expressed as:

$$\omega_0 = \sqrt{\frac{g_{mF1} g_{mS1}}{C_1 C_2}} \tag{41}$$

The sensitivities of ω_0 with regard to active and passive components are derived as:

$$\left.\begin{aligned} S_{g_{mS2}}^{\omega_0} &= S_{g_{mF2}}^{\omega_0} = S_{C_3}^{\omega_0} = 0 \\ S_{g_{mF1}}^{\omega_0} &= S_{g_{mS1}}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = \frac{1}{2} \end{aligned}\right\} \tag{42}$$

Therefore, from the above equation, it can be ensured that all the sensitivities for the oscillator circuits are low and do not exceed half in magnitude, which implies attractive sensitivity performances.

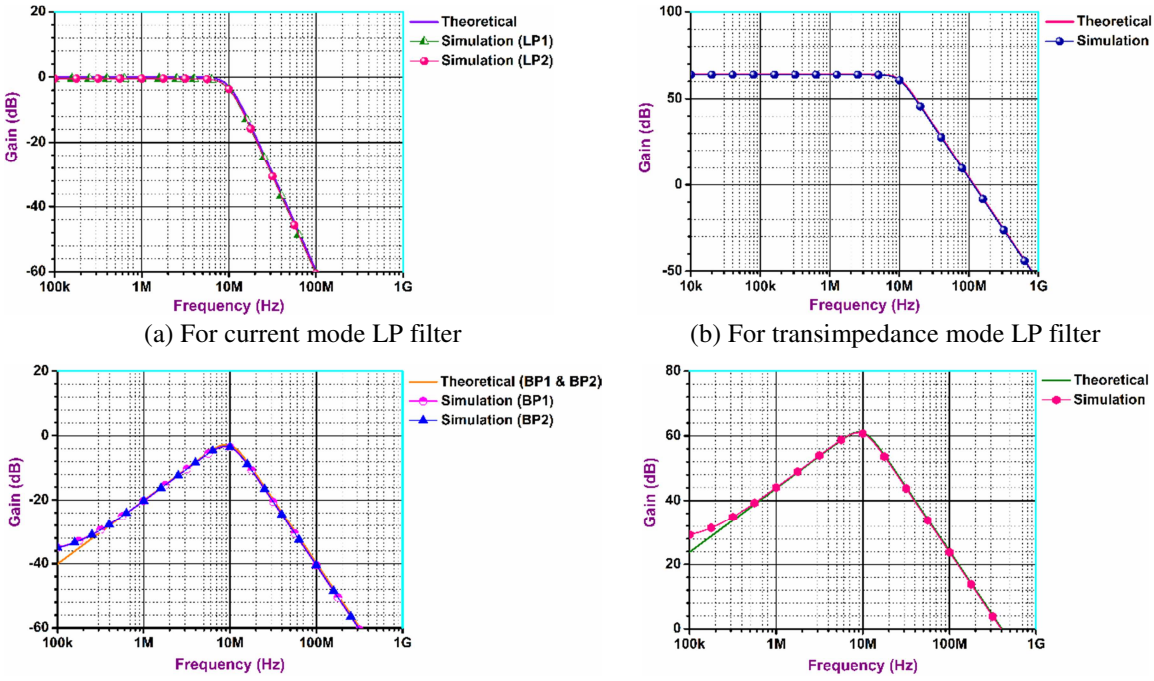
6. Simulation Results

PSPICE simulations are carried out to demonstrate the workability of the proposed circuits. The CMOS based VDTA block (shown in Fig. 2) is simulated with TSMC CMOS 0.18 μm technology parameter and a DC supply voltage of ±0.9 V. The aspect ratios of the transistors are taken as 3.6/0.36 for M1-M4 and 16.64/0.36 for M5-M8.

6.1. Simulation results of filter

For PSPICE simulation of the filter, the bias currents are selected as $I_{BF1} = I_{BF2} = I_{BS1} = I_{BS2} = 150$ μA ($g_{mF1} = g_{mF2} = g_{mS1} = g_{mS2} = 0.623$ mA/V), and the values of capacitors are selected as $C_1 = C_2 = C_3 = 10$ pF. The total power consumption is about 1.08 mW. Fig. 10 shows the theoretical and simulated frequency response of the current mode and the transimpedace mode filters with the appropriate selection of inputs and outputs according to Table 1. Figs. 10(a)-(d) depict the frequency response of current mode LP, transimpedance mode LP, current mode BP and transimpedance mode BP filters. The theoretical and simulated phase responses of these filters are shown in Figs. 11(a)-(d) respectively.

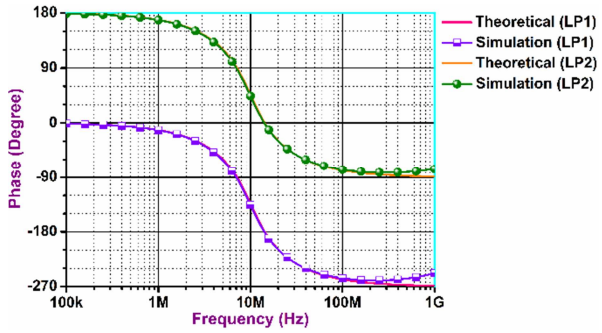
To illustrate the tuning property, BP1 and BP3 are chosen. By changing the bias current of VDTA, the values of f_0 are tuned to a particular Q value ($Q = 0.942$). For controllability of f_0 value, all the transconductance gains of the VDTA are set to be equal ($g_m = g_{mF1} = g_{mF2} = g_{mS1} = g_{mS2}$ or $I_B = I_{BF1} = I_{BF2} = I_{BS1} = I_{BS2}$) and varied to the values of 343 μA/V ($I_B = 50$ μA), 512 μA/V ($I_B = 100$ μA), 623 μA/V ($I_B = 150$ μA), 704 μA/V ($I_B = 200$ μA), 768 μA/V ($I_B = 250$ μA), and 824 μA/V ($I_B = 300$ μA). The graphs for BP1 and BP3 filters are shown in Fig. 12(a) and Fig. 12(b) respectively.



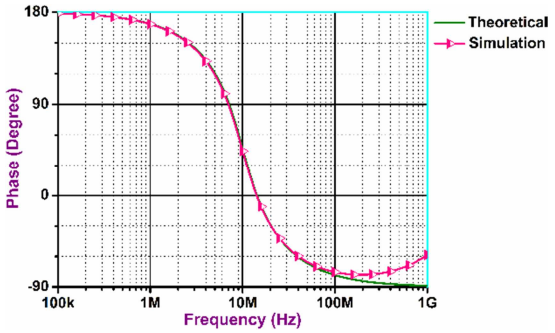
(a) For current mode LP filter (b) For transimpedance mode LP filter

(c) For current mode BP filter (d) For transimpedance mode BP filter

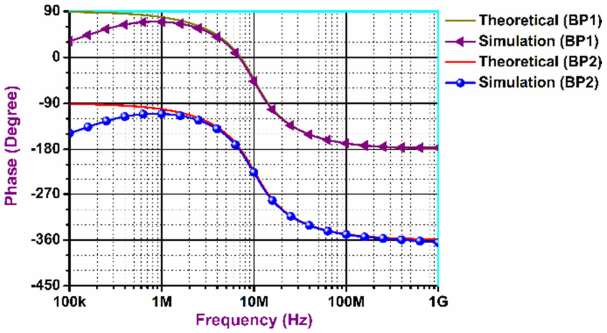
Fig. 10 Ideal and simulated frequency responses



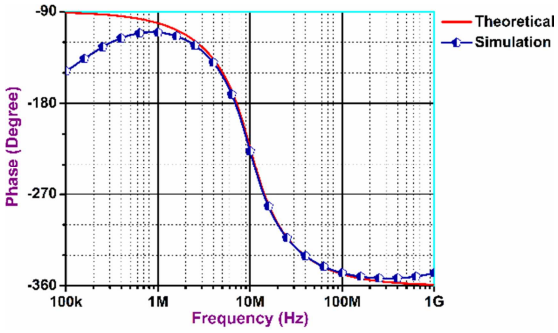
(a) For current mode LP filter



(b) For transimpedance mode LP filter

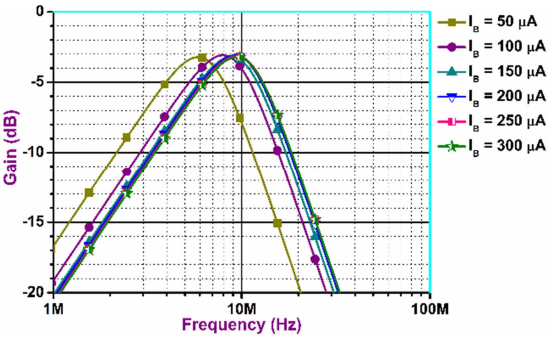


(c) For current mode BP filter

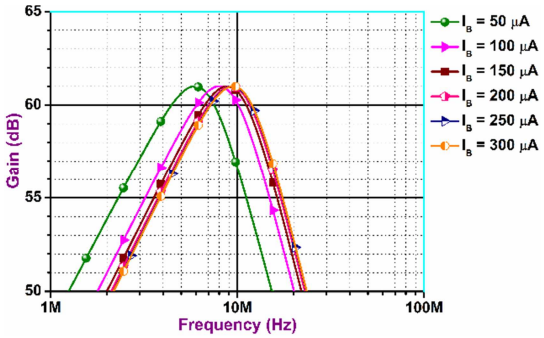


(d) For transimpedance mode BP filter

Fig. 11 Ideal and simulated phase responses



(a) For BP1 filter



(b) For BP3 filter

Fig. 12 Simulated responses using different bias current

The total harmonic distortion (THD) analysis is done for the BP1 filter to determine the quality of the output. The simulated THD values for the reported third order filter configuration are depicted in Fig. 13. It is concluded that the output distortion is within 2.06% for sinusoidal input currents up to 60 µA (peak). The intermodulation distortion (IMD) of the BP1 filter is investigated. Fig. 14 depicts the dependence of the 3rd IMD of BP1 response employing two nearly spaced tones f_1 = 8.71 MHz and f_2 = 9.11 MHz (0.2 MHz higher and lower frequencies than the center frequency of the BP filter) with the same input signal amplitude. It is observed that the 3rd IMD is 6.7% for input signals of 35 µA (peak). Hence, the output is of good quality and the dynamic range is large.

A final point deals with the impact of the active and passive discrepancies between the filter's frequency responses. Monte-Carlo analysis is conducted to collect statistical data. The BP1 filter is simulated by setting 5% tolerance for all the capacitors and also 5% variation for the dimension of the metal oxide semiconductor (MOS) transistors channel length. After one hundred simulation runs, the obtained statistical histogram is shown in Fig. 15. According to the simulation, f_0 value of the filters is affected in the range of −5.8% to +5.4% with a mean value of 8.90689 MHz and a standard deviation of 208.175 kHz. Thus, it is evident from the analysis results that the proposed third order filter topology has excellent sensitivity performance.

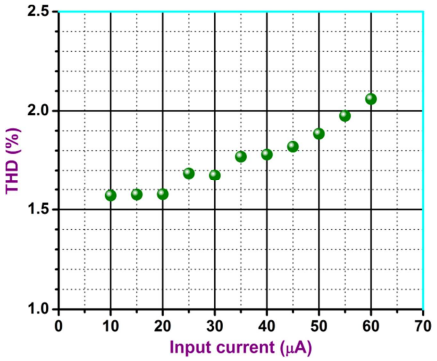


Fig. 13 Variation of THD against amplitude of input current

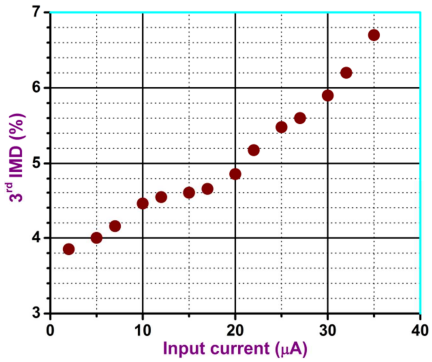


Fig. 14 Dependence of the third-order IMD of the BP1 filter on input current

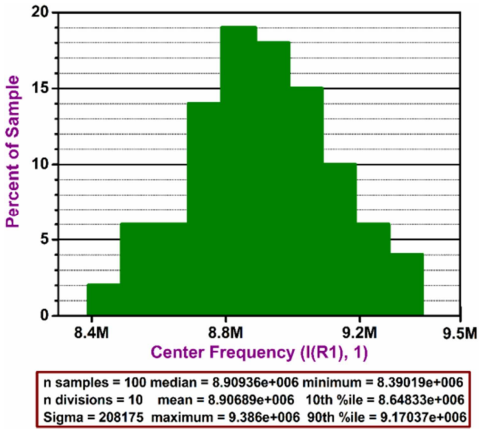


Fig. 15 Monte-Carlo analysis for the BP1 filter

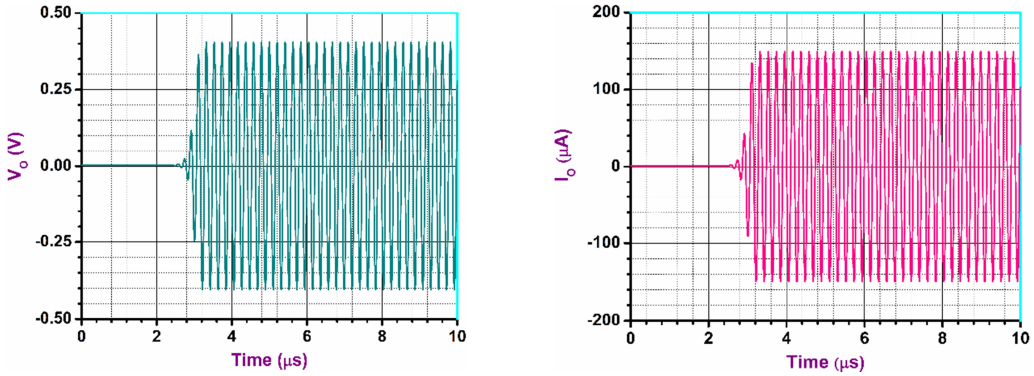
6.2. *Simulation results of oscillator*

A sinusoidal third order oscillator circuit is derived by making minor modifications to the reported filter configuration. This circuit is capable of producing outputs in both voltage and current modes. The biasing currents are selected as $I_{BF1} = I_{BF2} = I_{BS1} = I_{BS2} = 150$ μA and the values of all capacitors are chosen at 20 pF. To get the current output, a 330 Ω resistor is used at the output current node. The power dissipation is found to be 1.08 mW. Fig. 16 depicts the transient analysis of voltage and current outputs. These show the rise of oscillations and later attain a stable output. The corresponding steady state outputs are shown in Fig. 17. Simulation results show that the oscillation frequency is 4.77 MHz, which is close to the theoretical frequency of 4.96 MHz. The deviation is 3.83%.

The voltage and current output spectrums are shown in Fig. 18. The THDs for voltage (V_O) and current output (I_O) are 1.51% and 1.72% respectively. Fig. 19 shows the variations of THD against the amplitude of the biasing current. It is found that, for the entire current range, the THD value of the V_O varies from 1.12% to 1.98%, whereas it varies from 1.34% to 2.17% for the I_O. Fig. 20 shows the simulated dependence of the voltage and current output amplitude on bias current I_{BS1}. Fig. 20 confirms that the output voltage is almost constant for a bias current between 100 μA and 250 μA, whereas the output current is almost constant for a bias current between 50 μA and 250 μA.

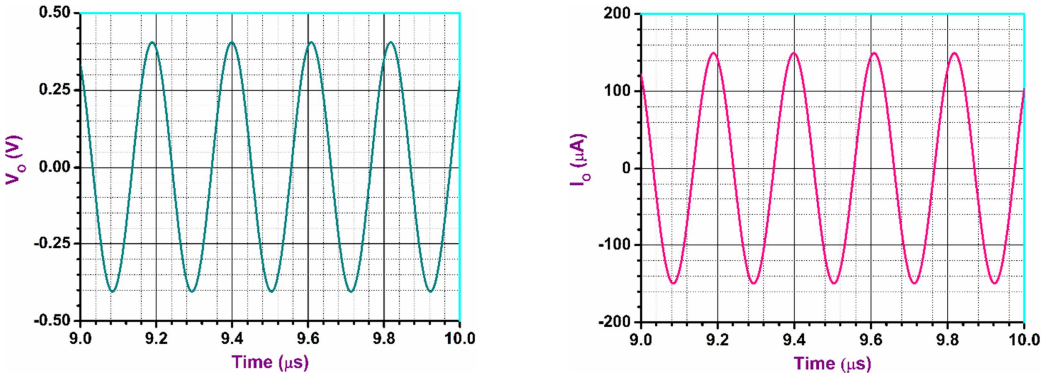
From Eq. (13) it is seen that the frequency of oscillation can be tuned with the help of a bias current (I_{BS1}) and a capacitor (C_2) without affecting CO. The variation in oscillation frequency with regard to bias current (I_{BS1}) and capacitor (C_2) are shown in Fig. 21. In Fig. 21(a), capacitor values are set at 20 pF and the bias current (I_{BS1}) is varied from 10 μA to 300 μA. The variation in frequency with the capacitor C_2 is obtained by changing the values of the capacitor C_2 from 1 pF to 10 nF and fixing the bias currents at 150 μA. For better clarity of the graph, the variation of frequency with the value of C_2 up to 100 pF is shown in Fig. 21(b). The measured highest and lowest frequencies are 20.554 MHz and 219.191 kHz respectively.

The robustness of the reported oscillator is checked through Monte-Carlo analysis with ±5% Gaussian deviation on capacitors. The histogram for 100 runs is depicted in Fig. 22. According to the obtained results, with a variation of FO between 3.93 MHz and 5.13 MHz, the f_0 value of the oscillator are affected in the range of –10% to +17%. It illustrates that the proposed oscillator exhibits reasonable sensitivity performance.



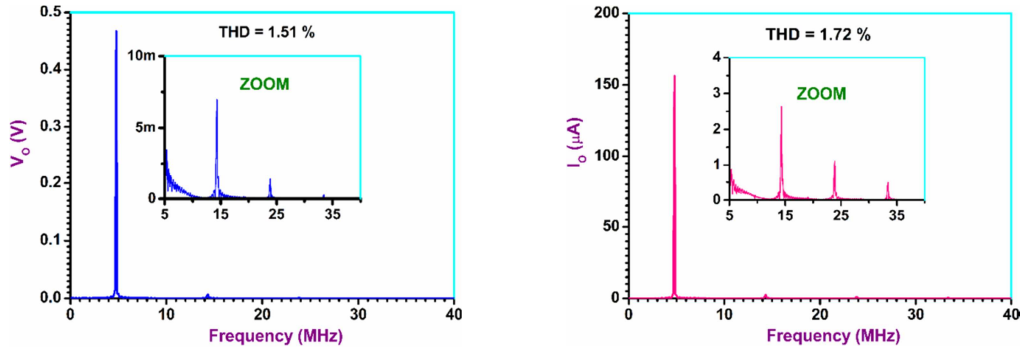
(a) For voltage (V_O) (b) For current (I_O)

Fig. 16 Transient response



(a) For voltage (V_O) (b) For current (I_O)

Fig. 17 Simulated waveforms in the steady state



(a) For voltage (V_O) (b) For current (I_O)

Fig. 18 The simulated frequency spectrum of the output waveforms

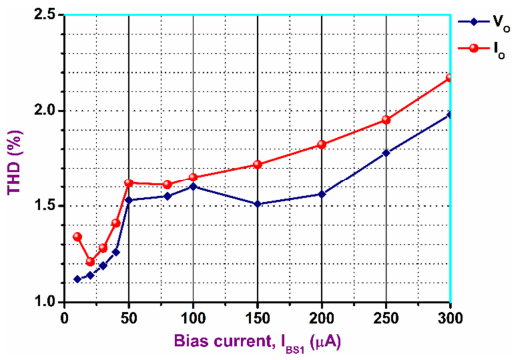


Fig. 19 Variation of THD (%) with I_{BS1}

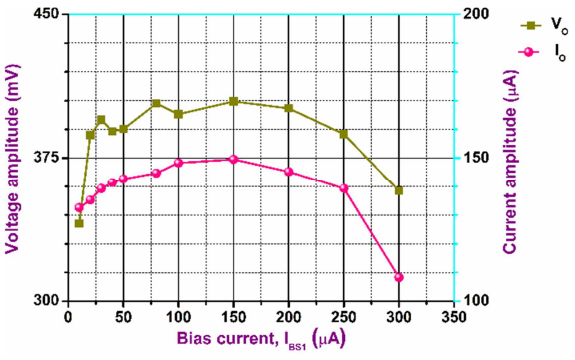
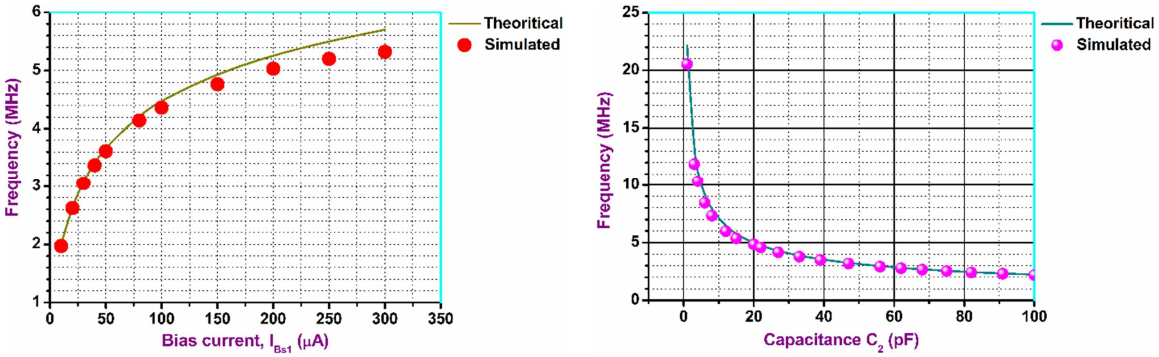


Fig. 20 Output amplitude versus I_{BS1}



(a) With bias current I_{BS1} (b) With capacitor C_2

Fig. 21 Frequency tuning

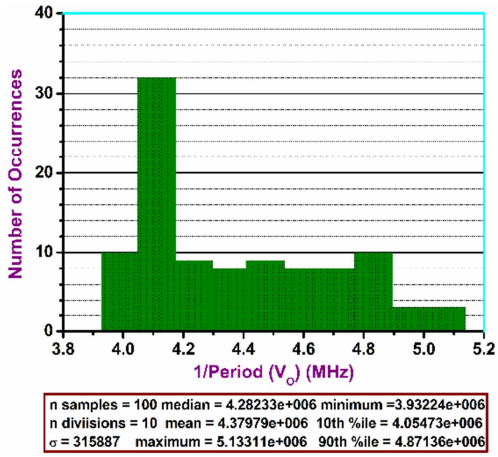


Fig. 22 Histogram of the reported oscillator after Monte Carlo simulation

7. Experimental Results

The simulation and experimental (using LM13700 IC) verification results for the third order filters and oscillator are studied next. Though the VDTA is not an off-the-shelf component, it can be implemented using commercially available ICs, i.e., LM13700. The practical implementation of VDTA using LM13700 IC is shown in the schematic of Fig. 23. Supply voltages of ±15 V and bias current 0.5 mA (g_m = 9.229 mA/V) are selected for both the simulation and experimental verification. The similarity is kept to appreciate comparison between simulation and hardware results.

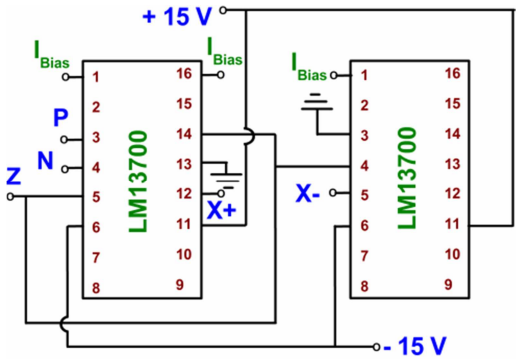
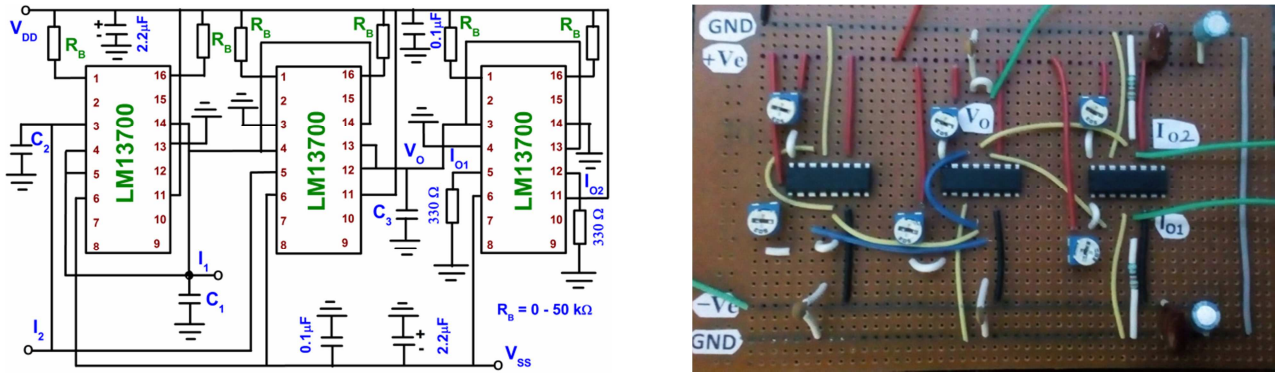


Fig. 23 VDTA realization using LM13700

7.1. Experimental results for third order filter

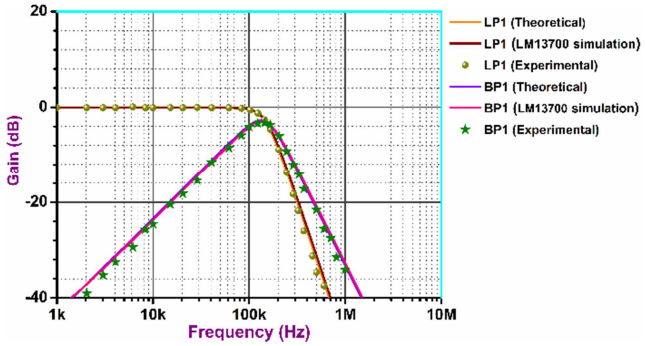
For hardware implementation, METRAVI multiple power supply (RPS3002-2), RIGOL function generator (DG1022), and AGILENT oscilloscope (350 MHz, 54641A) are used. To verify the proposed filters experimentally, the value of capacitors are selected as $C_1 = C_2 = C_3 = 10$ nF. Fig. 24(a) shows the schematic diagram of the realization of the proposed filter configuration of Fig. 3 using discrete components, and the actual hardware arrangement is depicted in Fig. 24(b). The

theoretical, simulation, and experimental (using LM13700 IC) results for the filters are shown in Fig. 25. It is concluded from the figures that though small deviations are observed in the experimental result, the simulation results are close to the theoretical results. For controllability of the f_0 value, all the transconductance gains of VDTA are set to be equal ($g_m = g_{mF1} = g_{mF2} = g_{mS1} = g_{mS2}$ or $I_B = I_{BF1} = I_{BF2} = I_{BS1} = I_{BS2}$) and varied to the values of 9.229 mA/V (I_B = 0.5 mA), 10.893 mA/V (I_B = 0.6 mA), and 12.575 mA/V (I_B = 0.7 mA). The corresponding graph for BP1 filter is depicted in Fig. 26.

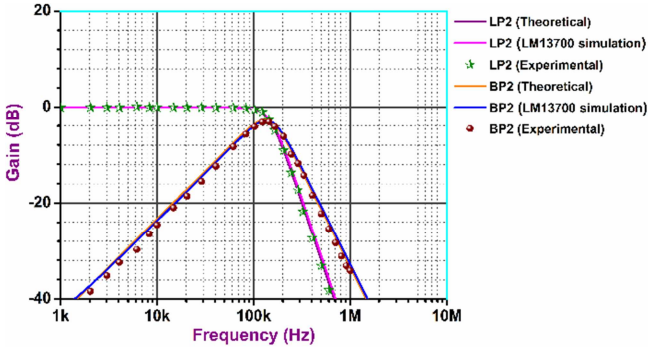


(a) Schematic diagram (b) Experimental setup

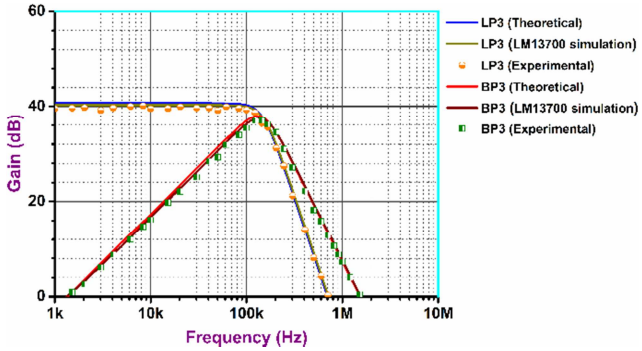
Fig. 24 Experimental arrangement for the recommended third order filters



(a) For non-inverting current mode filter



(b) For inverting current mode filter



(c) For transimpedance mode LP/BP filter

Fig. 25 Ideal, simulated, and experimental frequency responses

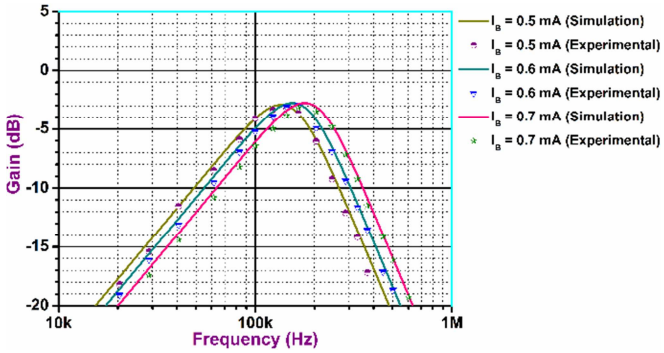
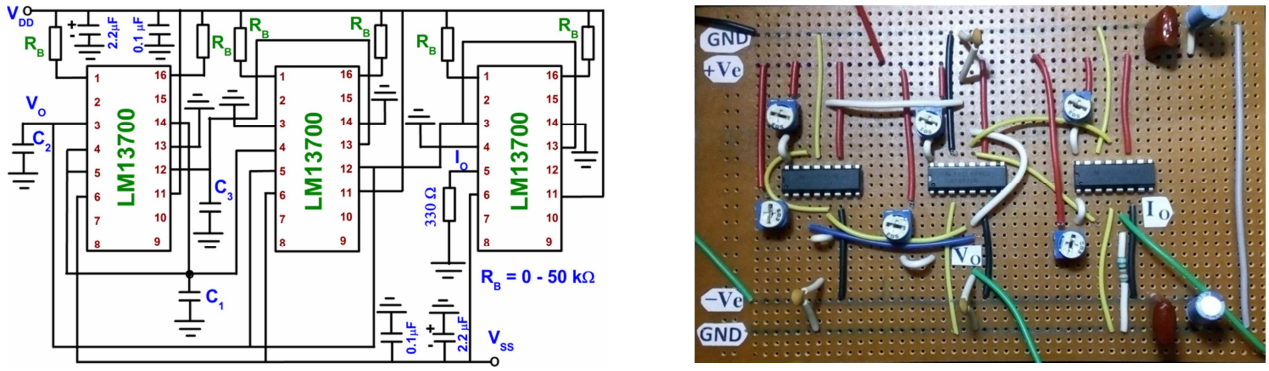


Fig. 26 Simulated and experimental responses using different bias currents for BP1 filter

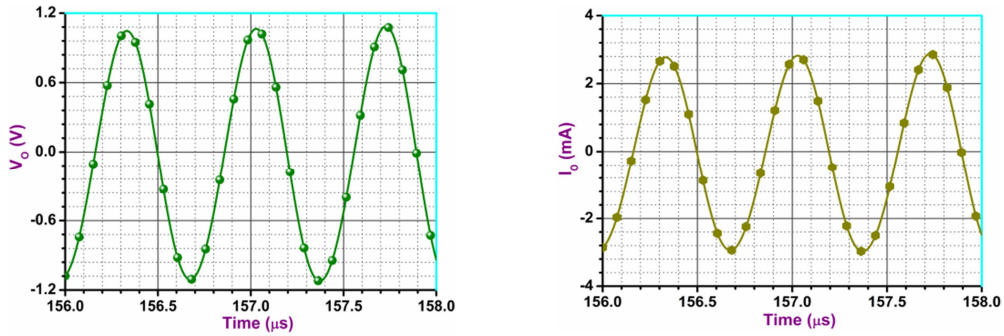
7.2. Experimental results for third order oscillator

For experimental verification of the proposed third order oscillator, the value of capacitors are selected as $C_1 = C_2 = C_3 =$ 1 nF. This choice leads to an oscillation frequency of 1.469 MHz. With these values, the condition of oscillation is satisfied. The circuits are supplied with METRAVI multiple power supply (RPS3002-2). AGILENT oscilloscope (350 MHz, 54641A) is used to observe the oscillations. The schematic diagram and the experimental arrangement on veroboard for evaluating the behavior of the recommended oscillator configuration are demonstrated in Fig. 27. The simulation results (using LM13700 IC) for the proposed oscillator are demonstrated in Fig. 28. The 330 Ω resistor load is used to convert the output current into voltage at the output current node. It is justified from Fig. 28 that as claimed earlier, the proposed configuration is capable of generating voltage (V_O) and current (I_O) waveforms. The measured oscillation frequency in Fig. 28 is 1.432 MHz, which is close to the theoretical value, and the error rate is 2.5%. The experimental (using LM13700 IC) voltage and current outputs are shown in Fig. 29(a) and Fig. 29(b), respectively. The figure depicts that the yield frequency is 1.356 MHz, which is an error of 7.7%. In order to focus on comparative study among theoretical, simulation, and experiment values, a curve between varying values of bias current (I_{BS1}) and frequency of oscillation is drawn and presented in Fig. 30. This graph shows the deviation between frequency values obtained in all three cases for a fixed value of I_{BS1}.



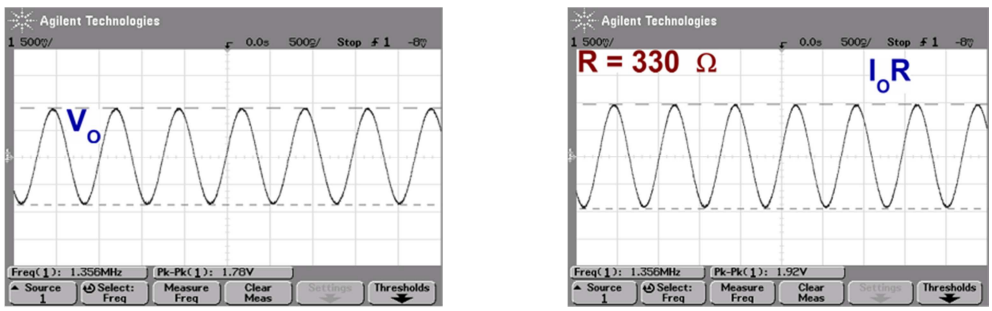
(a) Schematic diagram (b) Experimental setup

Fig. 27 Experimental setup for the recommended third order oscillator



(a) For voltage (V_O) (b) For current (I_O)

Fig. 28 Simulated waveforms in the steady state using LM13700



(a) For voltage (V_O) (b) For current (I_O)

Fig. 29 Experimental waveforms in the steady state using LM13700

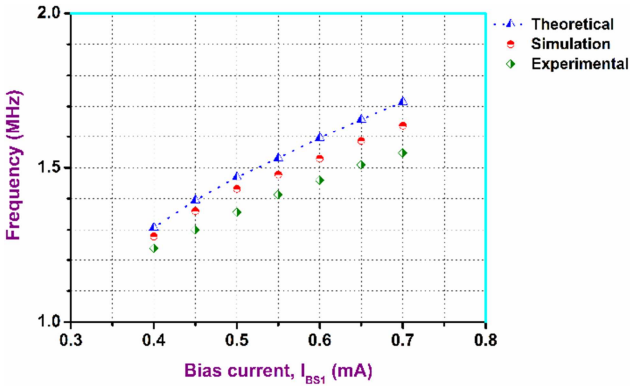


Fig. 30 Variations in frequency of oscillation with respect to I_{BS1}

8. Comparison with Existing Structures

The proposed VDTA based filters are compared with different third order filters and presented in Table 2. Third order analog filters using various types of active elements are well known to be of greater interest than second order filter, as they can be used where a sharp cut off is desired and also being useful to implement digital filters. Though only the LP and BP filter responses can be realized in this configuration, the proposed filter circuit has various advantages over the previously reported third order filters. A summary of this comparison is shown below:

(1) The proposed filter circuit uses two VDTA blocks in contrast to the work of [10-11, 16-21, 23, 25] which require more than two active blocks.

(2) In the work of [9-10, 12-16, 20, 22-24], numerous passive elements are required in contrast to the reported circuit which requires only three capacitors.

(3) The proposed filter circuit realizes current mode and transimpedance mode LP and BP filters without any matching conditions in comparison to the work of [9, 11, 13, 15, 24].

(4) The proposed filter circuit requires a low supply voltage in comparison with the work of [10-14, 18, 23-25] which need a comparatively large supply voltage.

(5) Moreover, all the capacitors employed in the reported circuit are grounded in comparison to the work of [12-15, 24-25].

(6) Additionally, the reported circuit has a tuning capability whereas the circuits in the work of [9-10, 12-17, 21-24] cannot be tuned electronically.

In comparison to the above-mentioned work, the designed third order filter uses only two active devices along with all the grounded capacitors. It can be tuned electronically through the bias currents of VDTA. Moreover, there is no requirement for matching conditions to obtain filter responses. It is evident that all the above advantages cannot be simultaneously achieved in any of the work reported in Table 2, thus justifying our design proposal.

The proposed oscillator is compared with previously reported VDTA based third order oscillators and presented in Table 3. The third order sinusoidal oscillators offer better frequency response and low harmonic distortion than second order oscillators. A summary of this comparison is listed below:

(1) The proposed oscillator does not require multiple output terminals of ABBs compared to all the above VDTA based reported circuits [26-29].

(2) Comparatively large supply voltages are needed for the oscillator reported in the work of [26-27] compared to the proposed oscillator.

(3) Moreover, the proposed third order oscillator can be realized without any matching condition in comparison to the work of [26].

Table 2 Comparison of the proposed filter with the previously developed third order filters

Ref.	Analog blocks used	External capacitors and resistors required	Availability of inbuilt tuning	Power consumption (mW)	Types of responses available	Sensitivity/ THD	Technology	Supply voltage (V)	Mode of operation	Matching condition	Noise analysis	Experimental results
[9]	Fig. 1 1 DBTA, 1 AD844	3 (G) + 5 (3 G, 2 F)	No	Not reported	LP	Not reported	AD844	±12	Voltage	Yes	Not reported	Yes
[10]	Fig. 4(a) 8 CFTA	4 (G) + 0	No	Not reported	LP	Not reported	0.35 µm	±1.65	Voltage	No	Not reported	Yes
[11]	Fig. 3 3 CCCII	3 (G) + 0	Yes	25.6 [25]	BP	–/3.43% [25]	0.35 µm	±2.5	Voltage	Yes	Total output noise voltage at center frequency 11.482 MHz is 5.845 nV/√Hz, equivalent input noise voltage 14.782 nV/√Hz.	No
[12]	Fig. 3 2 CDBA	5 (1 G, 4 F) + 5(1 G, 4 F)	No	Not reported	AP	≤1/–	Level-3	±5	Current	No	Not reported	No
[13]	Fig. 9 1 CDBA Fig. 10 1CDBA	3 (1 G, 2 F) + 4 (1 G, 3 F) 3 (1 G, 2 F) + 3 (1 G, 2 F)	No	Not reported	LP and BP	$-\frac{1}{3}$/–	0.25 µm	±1.25	Voltage	Yes No	Not reported	No
[14]	Fig. 4 1 CDBA	4 (1 G, 3 F) + 5 (1 G, 4 F)	No	Not reported	LP	$\leq-\frac{1}{2}$/–	3 µm	±5	Voltage	No	Not reported	No
[15]	Fig. 1 1 CDBA, 1 CFA	3 (2 G, 1 F) + 7 (4 G, 3 F)	No	Not reported	LP	≤1/–	AD844	±12	Voltage	Yes	Not reported	Yes
[16]	Fig. 4 5 CDBA	3 (G) + 12 (2 G, 10 F)	No	1590 [29]	AP	–/0.273 [25]	AD844	±12	Current	No	Total output noise voltage at 15.9 kHz frequency is 480 nV/√Hz and equivalent input noise is 49.17 pA/√Hz [25].	Yes
[17]	Fig. 3 3 OTA	3 (G) + 0	No	0.006	LP	Not reported	0.18 µm	±0.5	Current	No	Not reported	No
[18]	Fig. 3 4 DO-OTA Fig. 4 6 DO-OTA	3 (G) + 0	Yes	Not reported	BP	≤1/–	0.5 µm	±2	Current	No	Not reported	No
[19]	Fig. 1 4 OTA, 3 OA	0 + 0	Yes	Not reported	HP and LP	≤1/–	Not reported	±10	Current	No	Not reported	No
[20]	Fig. 1 3 OA	0 + 10 (4 G, 6 F)	Yes	Not reported	HP	≤1/–	LF 356N	±18	Current	No	Not reported	No
[21]	Fig. 1 3 OP-AMPA, 8 MOSFET	3 (G) + 0	No	Not reported	HP, LP, and BP	$\leq\frac{1}{3}$/–	µA741	±22	Voltage	No	Not reported	No
[22]	Fig. 1 2 CFA	3 (G) + 6 (5 G, 1 F)	No	Not reported	LP	$\leq\frac{1}{27}$/–	AD844	±12	Voltage	No	Not reported	Yes
[23]	Fig. 5 4 MOCCII	3 (G) + 4 (3 G, 1 F)	No	7.54 [25]	HP, LP, BP, BR, and AP	≤1/1.54 [29]	0.18 µm	±1.25	Current and transimpedance	No	Total output noise voltage at 3 kHz frequency is 28 nV/√Hz and equivalent input noise is 14 pA/√Hz [25].	No
[24]	Fig. 4 1 OTRA	6 (F) + 5 (F)	No	1.73 [25]	HP, LP, BP, BR, and AP	$-\frac{1}{3}$/4.5%	0.5 µm	±1.5	Voltage	Yes	Total output noise voltage is 0.13 nV/√Hz and equivalent input noise is 0.1253 nA/√Hz at 200 kHz frequency [25].	No
[25]	Fig. 3 3 CCCII	3 (F) + 0	Yes	56.9	HP, LP, BP, BR, and AP	≤0.4/3.25	0.35 µm	±2.5	Voltage	No	Total output noise voltage at 1 MHz frequency is 3.856 nV/√Hz and equivalent input noise is 4.092 nV/√Hz.	No
This work	Fig. 3 2 VDTA	3 (G) + 0	Yes	1.08	LP and BP	≤0.5/2.06	0.18 µm	±0.9	Current and transimpedance	No	Total output noise voltage at 10 MHz frequency is 4.81 nV/√Hz and equivalent input noise is 5.926 pA/√Hz.	Yes

Note: G = grounded; F = floating; HP = high-pass; BR = band-rejection; AP = all-pass; DBTA = differential buffered and transconductance amplifier; CFTA = current follower transconductance amplifier; CCCII = current-controlled current conveyor; CFA = current feedback amplifier; DO-OTA = Dual-Output operational transconductance amplifier; OA = operational amplifiers; MOCCII = multiple output second-generation current conveyor; OTRA = Operational transresistance amplifier.

Table 3 Comparison of the proposed oscillator with available VDTA based third order oscillators

Ref.	Number of VDTA used	Number of resistor used	Number of capacitor used	Need of ABB with multiple output terminals	Electronic tuning FO without disturbing CO	Need of matching condition	Use of grounded capacitor	Technology	THD/ Sensitivity	Supply voltage (V)	Power consumption (mW)	Output type	Experimental results
[26]	2	0	3	Yes	Yes	Yes	Yes	0.35 µm	≤1.8/0.5	±2	Not reported	Both	No
[27]	2	0	3	Yes	Yes	No	Yes	0.25 µm	≤2.98%/–	±1	Not reported	Both	No
[28]	2	0	3	Yes	Yes	No	Yes	0.18 µm	≤3.29%/–	±0.9	0.457	Both	Yes
[29]	2	0	3	Yes	Yes	No	Yes	0.18 µm	≤4.5%/0.5	±0.9	Not reported	Both	Yes
The proposed oscillator	2	0	3	No	Yes	No	Yes	0.18 µm	≤2.17%/0.5	±0.9	1.08	Both	Yes

Table 3 presents the various features of the previously reported VDTA based oscillator. However, none of them can be realized without the use of additional copy terminals of VDTA. The proposed oscillator is composed of two VDTAs and three grounded capacitors, without requiring resistors. Although the quadrature outputs are not available in the oscillator, it has a voltage mode and a current mode sinusoidal output. The CO and FO of the oscillator can be tuned electronically. Furthermore, no matching conditions are required. Hence, the proposed circuit is strikingly superior to others compared here.

9. Conclusions

A third order resistorless filter circuit that provides current mode and transimpedance mode LP and BP filters without any matching condition is presented in this work. By selecting the input and output terminals properly, the filter responses can be obtained without changing the circuit topology. By making minor modifications to the third order filter configuration, sinusoidal oscillator configuration can be easily realized as it has supporting advantageous features, e.g., resistorless approach, use of grounded capacitors, availability of voltage and current outputs explicitly, orthogonally and electronically tunable condition of oscillation and frequency of oscillation, etc. The PSPICE simulation results using 0.18 µm CMOS technology and experimental results confirm the desired performance of the proposed filters and oscillator. Additionally, non-ideal and sensitivity analysis is also included. The simulation results confirm that the power dissipation is 1.08 mW for both circuits, whereas THDs are less than 2.06% up to 60 µA and 2.17% up to 300 µA for the filter and oscillator circuits, respectively. For the filter, the IMD is less than 6.7% up to 35 µA input signals. For the oscillator, the output voltage is almost constant for a bias current between 100 µA and 250 µA, whereas the output current is almost constant for a bias current between 50 µA and 250 µA. Therefore, the proposed third order filters and oscillator may bring an effective alternative to the arena of third order filter and oscillator design for researchers.

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Conflicts of Interest

The authors declare no conflict of interest.

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