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IMPLEMENTATION OF DYNAMIC RANGE CONTROLLER ON DIGITAL SIGNAL PROCESSOR

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The aim of this work was to build a real time digital range controller which could be used in the radio and television recording and broadcasting studios. The main purpose of the system is to change the dynamic range of an audio signal in a predefined way without introducing perceptible distortions, what guarantees an optimal use of the overall available dynamic range of an audio system. As a processor, the ADSP-21065L digital signal processor manufactured by Analog Devices was used. An input/output digital audio signal interface was designed and constructed using Atmega8L microcontroller manufactured by Atmel and FPGA device. The characteristics of the dynamic range controller were performed.

Keywords: dynamic range control, limiter, compressor, expander, noise gate, digital signal processing.

1. Introduction

Analogue or digital dynamic range control (DRC) is frequently used for recording, mixing, mastering and editing of audio signals, especially in radio and television production. The aim of DRC is to protect the equipment from overloads and to assure optimal use of all the dynamic range of recording systems. DRC is also used for artistic purposes.

Analogue dynamic range controllers usually work using variable-gain amplifiers, such as voltage controlled amplifiers or light sensitive diodes, to reduce the gain of a signal. Digital realization of DRC is much more flexible than analogue, and it allows precise changes to its characteristic parameters.

2. The dynamic range control algorithm

Dynamic range control is a process that changes the dynamic range of an audio signal in the predefined way. In most cases, it is performed using gain curve $g(n)$, derived

from the signal's level measurement and its static and dynamic characteristics. After input signal level X[dB] is measured, output level Y[dB] is changed by the factor of $g(n)$ according to equation (1), where $x(n-D)$ is the delayed input signal.

$$y(n) = g(n) \cdot x(n-D). \tag{1}$$

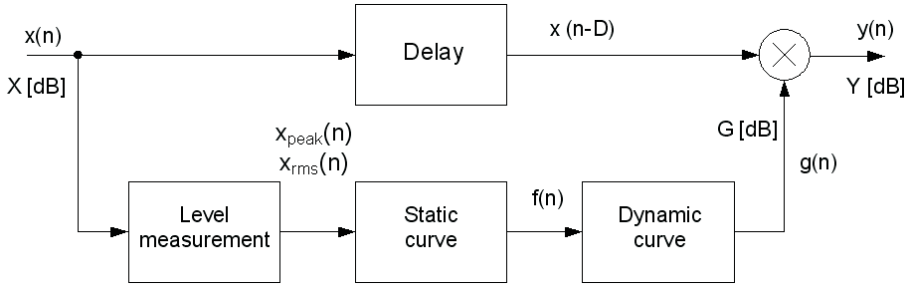

Fig. 1. Block diagram of typical DRC system.

To allow predictive control of the output level, the delay of the input signal $x(n)$ can be implemented. The attack time and the recovery time are specified accordingly to the IEC recommendation. The attack time was given as the time taken after a tone burst had been applied to an initial 6 dB overshoot to be reduced to within 2 dB of its initial value. The recovery time, sometimes called the decay or release time, is specified as the time taken for the output level to increase to within 2 dB of its final level. These two main time constants depend on the level detector and the dynamic characteristics implemented in the dynamic range controller.

According to level detection, two basic signal measure algorithms: peak (2) and RMS (3) detection were implemented in the digital signal processor. To get the autorecovery mode, the peak and RMS detection can be combined. Such realization offers a short recovery time for isolated peaks, but for signals of higher average level this parameter can be extended. Such solution prevents from excessive limiting or compression. Parameters *AT*, *RT* and *TAV* are related to the attack, recovery and averaging time constants as shown in equations (4), where T_s= 1/f_s is the sampling period of the input audio signal.

$$x_{\mathrm{PEAK}}(n) = (1-RT) \cdot x_{\mathrm{PEAK}}(n-1) + AT \cdot \mathrm{rect}\left(|x(n)| - x_{\mathrm{PEAK}}(n-1)\right), \tag{2}$$

$$x_{\mathrm{RMS}}(n) = x_{\mathrm{RMS}}(n-1) + TAV \cdot \left(x^2(n) - x_{\mathrm{RMS}}(n-1)\right), \tag{3}$$

where:

$$AT = 1 - e^{-2.2 \cdot T_S / t_{AT}}, \quad RT = 1 - e^{-2.2 \cdot T_S / t_{RT}}, \quad TAV = 1 - e^{-2.2 \cdot T_S / t_{TAV}}. \tag{4}$$

The relationship between input signal level $x(n)$ and gain-control signal $g(n)$ is defined by a static level curve shown in Fig. 2b. Figure 2a shows the output level in the function of the input level. The characteristic points in these figures are threshold

levels (*NT* – noise threshold, *ET* – expander threshold, *CT* – compression threshold, *LT* – limiter threshold), at which the required procedure of the dynamic range controller is executed.

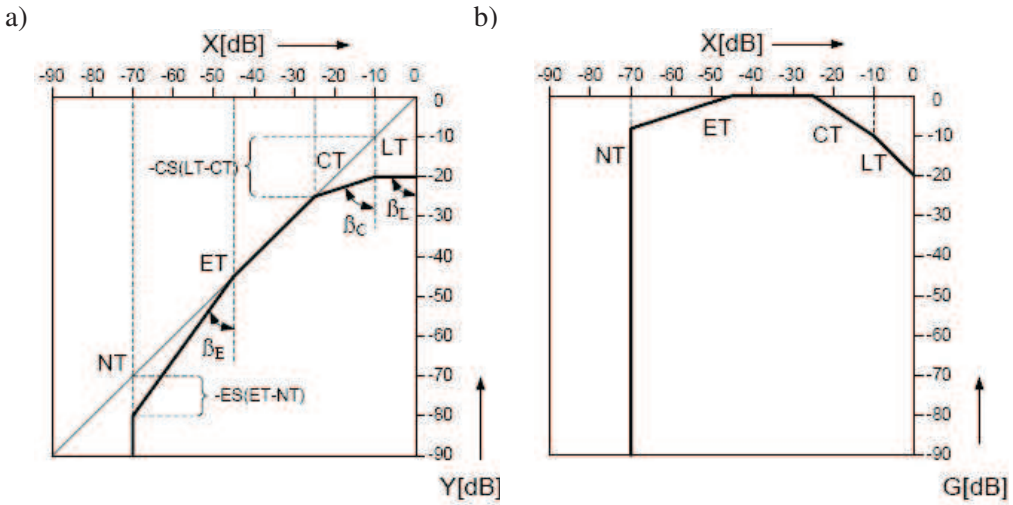

Fig. 2. Static characteristics of the dynamic range controller.

All thresholds marked in Fig. 2 are defined as the lower limit for the limiter and compressor and the upper limit for the expander and noise gate. Slope S of the output characteristics (Fig. 2a) is related to the tangent of the β angle which determines compression factor R. This describes the ratio between input and output levels of the dynamic range controller (4) as:

$$R = \frac{1}{1-S} = \tan\beta. \tag{5}$$

Since static characteristics are mostly defined in decibels, it is necessary to calculate logarithms and antilogarithms. Because of the complexity of this computation, two lookup tables were used. To reduce the amount of required storage, logarithm value x was calculated as shown in equation (5), where m is the mantissa and N is the exponent in the floating point representation of x.

$$\log_2(x) = \log_2(m \cdot 2^{-N}) = -N + \log_2 m. \tag{6}$$

Base 2 logarithms employed to simplify the operation of the conversion to and from base 10 logarithms are also implemented in the digital signal processor. Mantissa values should be scaled into a number between 0.5 and 1, thus the N shifts operation is performed. Because of a limited accuracy of the processing, the gain-control signal introduces zipper noise to the output signal. To diminish this influence, the gain factor smoothing was employed (Fig. 3). *AT* and *RT* could be the same factors as in the level detector, and are selected whether the gain-control signal is in the attack or release status.

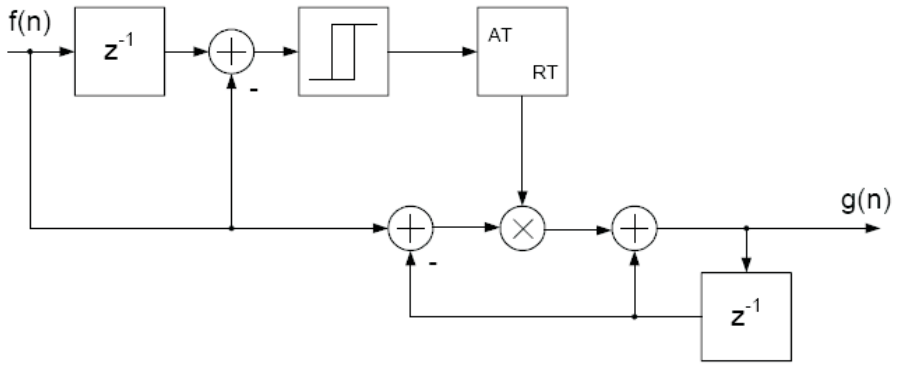

Fig. 3. Block diagram of gain smoothing implementation.

3. Interface card module

The interface card module was made as a separate circuit board connected to the EZ-LAB board using 96-pin EMAFE connector. As a digital signal processor, the ADSP-21065L manufactured by Analog Devices was chosen. The I/O digital audio signal interface was constructed by means of the Atmega8L microcontroller manufactured by Atmel and the FPGA device manufactured by Altera. Data transmission between the digital signal processor and the interface card was realized by means of two serial ports of the processor. One port is used to transmit and receive digital audio signals, and the other one serves for the communication between the interface card module and the signal processor. In order to transmit and receive digital audio signals in the AES3 standard, two AKM modules were implemented. Both of them have low jitter, good analog PLL synchronization and work with sampling rates from the range of 32 kHz to 192 kHz. Because of the similarity between AES/EBU and S/PDIF standards, both digital audio signal standards were implemented and the RCA and XLR connectors were used.

All parameters, such as thresholds, ratios and time constants can be selected via the user interface implemented in a microcontroller. To provide interaction with a user, six switches are used to select a proper menu item and to change the values of the dynamic range controller's parameters. The names of the parameters and their values are shown on a LED display. To project the level of the input and output audio signals, 8 LED diodes are used. Data transition between LED diodes, display, switches and the microcontroller is performed by means of serial buffers.

A digital audio signal from the AES3 receiver passes through the FPGA device to the digital signal processor. Then, a processing signal goes through the FPGA device to the AKM transmitter. The FPGA device is a signal router and a voltage volume adapter. It routes both audio and data signals from the microcontroller to the digital signal processor and audio signals between the receiver, transmitter and the signal processor.

4. Summary

The circuit board was designed and tested, and the software suitable for three programmable devices was developed. Subjective listening tests were carried out, and appropriate static characteristics were measured using System Two Cascade manufactured by Audio Precision. One of the typical static curve is shown in Fig. 4 with the following parameter values: $LT = -10\,\mathrm{dB}$, $CT = -20\,\mathrm{dB}$, $ET = -40\,\mathrm{dB}$, $NT = -80\,\mathrm{dB}$, and the compression and expansion ratio of respectively 2:1 and 1:2.

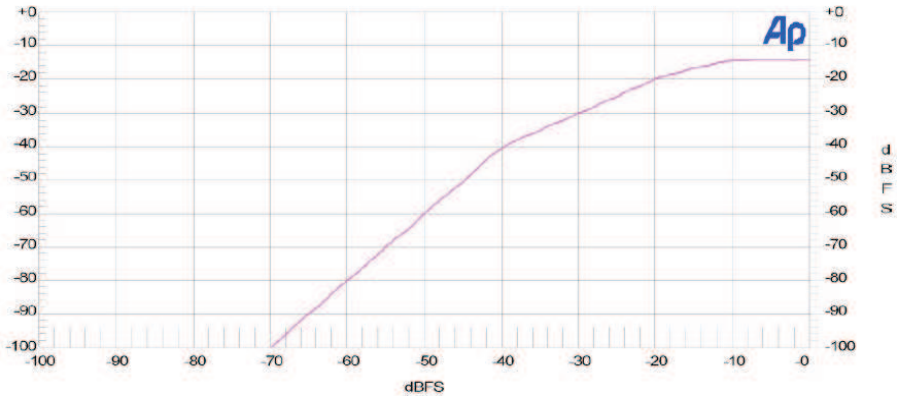

Fig. 4. Static characteristics of the dynamic range controller.

Dynamic characteristics were measured using 15 seconds samples with the tone burst. Test signals consisted of three phases. In the first one the level of the signal was below the threshold set up in the dynamic range controller. During the second phase the level was raised to full scale and the attack time was measured. During the last phase the level was reduced below the threshold and the release time was measured.

Digital signal controller can be use also for educational purposes. Easy to use interface and possibility of reconfiguration make this device suitable for students.

Further works should improve the DRC algorithm by the use of the overlapping method to reduce distortion of the processing signal.

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